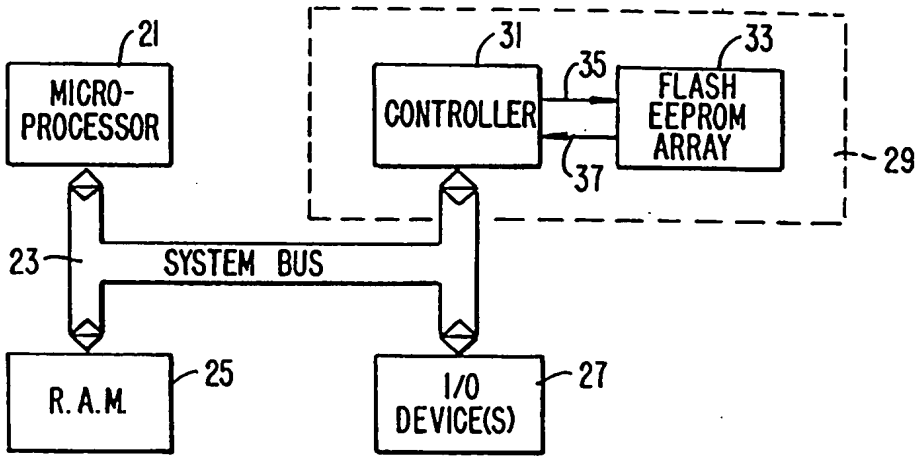

21
MICRO-
PROCESSOR
31
CONTROLLER
35
33
FLASH
EEPROM
ARRAY
37
29
23
SYSTEM BUS
R.A.M.
25
I/O
DEVICE(S)
27

FIG._1A

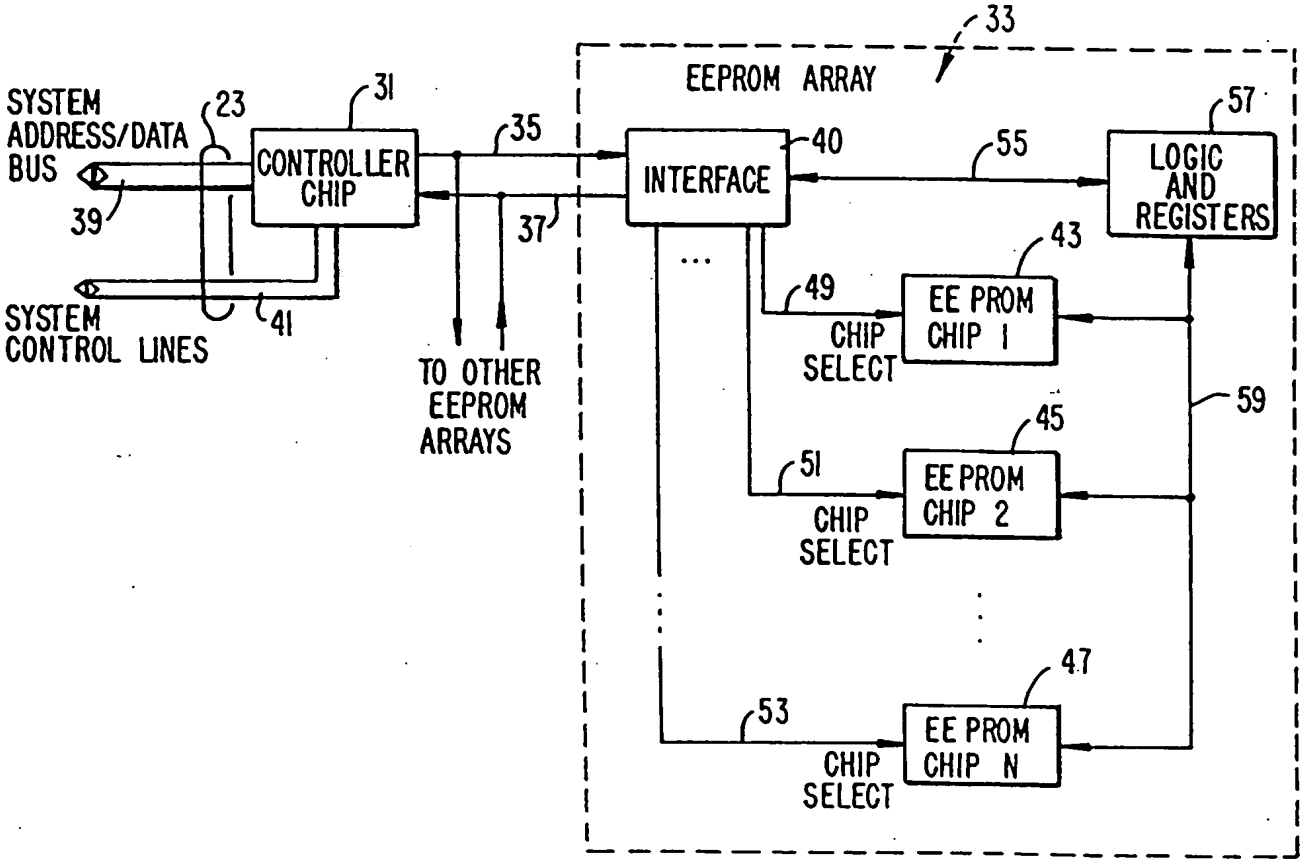

33
EEPROM ARRAY
SYSTEM
ADDRESS/DATA
BUS
23
31
CONTROLLER
CHIP
35
39
37
SYSTEM
CONTROL LINES
41
TO OTHER
EEPROM
ARRAYS
INTERFACE
40
55
57
LOGIC
AND
REGISTERS
43
49
CHIP
SELECT
EE PROM
CHIP 1
59
45
51
CHIP
SELECT
EE PROM
CHIP 2
47
53
CHIP
SELECT
EE PROM
CHIP N

FIG._1B

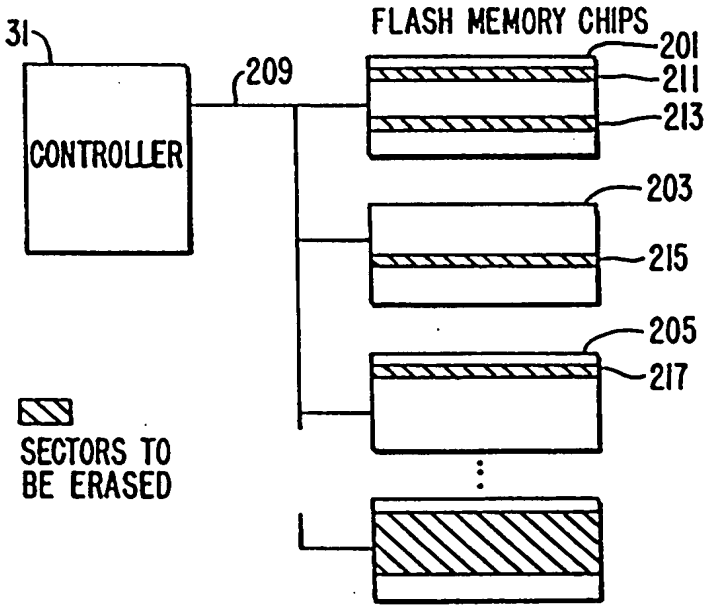


FIG._2

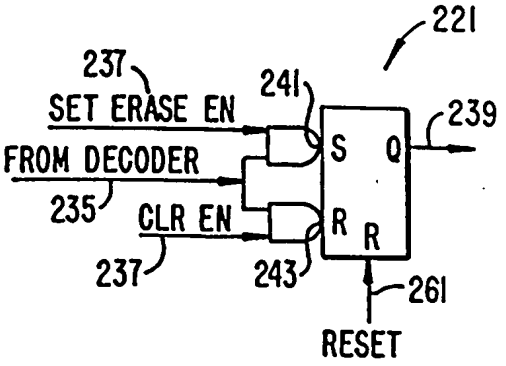


FIG._3B

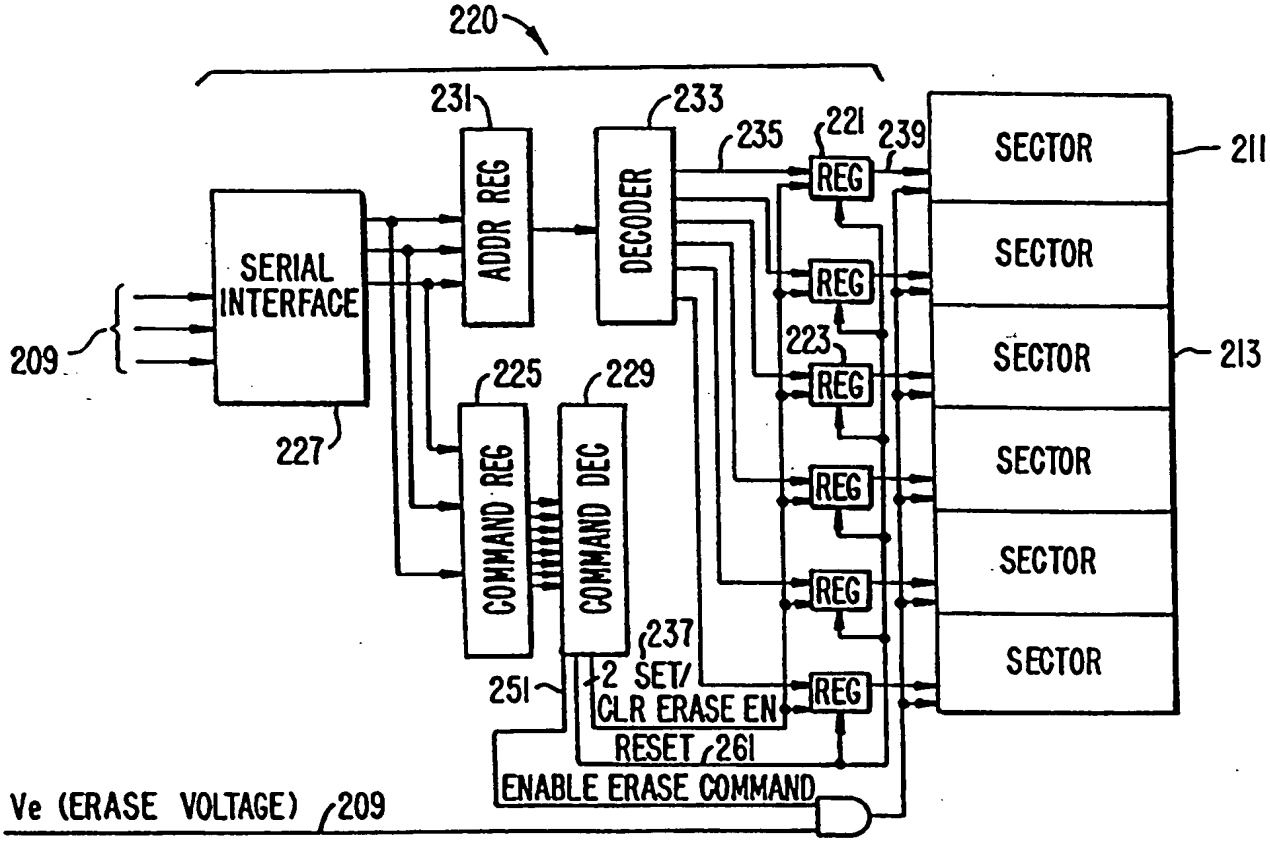


FIG._3A

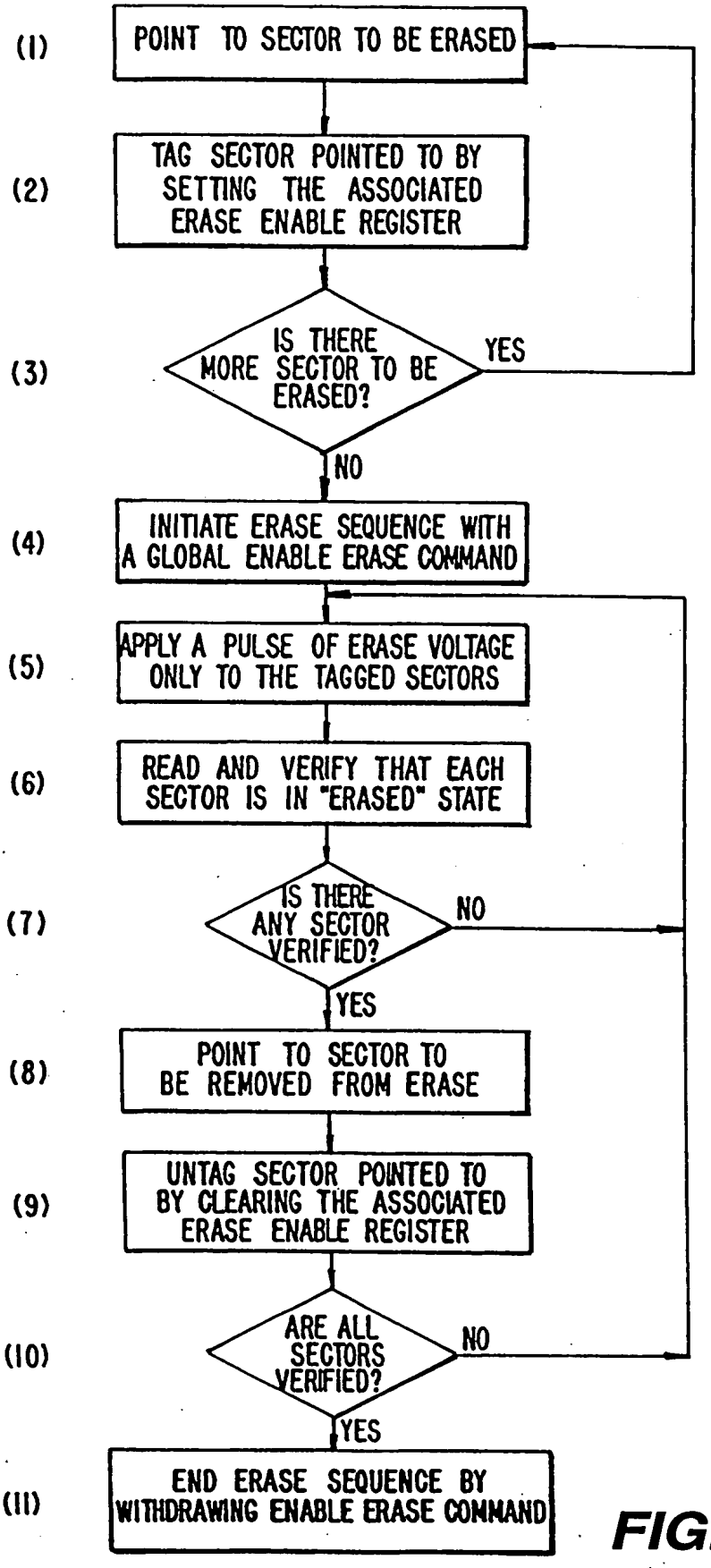

(1)
POINT TO SECTOR TO BE ERASED
(2)
TAG SECTOR POINTED TO BY SETTING THE ASSOCIATED ERASE ENABLE REGISTER
(3)
IS THERE MORE SECTOR TO BE ERASED?
YES
NO
(4)
INITIATE ERASE SEQUENCE WITH A GLOBAL ENABLE ERASE COMMAND
(5)
APPLY A PULSE OF ERASE VOLTAGE ONLY TO THE TAGGED SECTORS
(6)
READ AND VERIFY THAT EACH SECTOR IS IN "ERASED" STATE
(7)
IS THERE ANY SECTOR VERIFIED?
NO
YES
(8)
POINT TO SECTOR TO BE REMOVED FROM ERASE
(9)
UNTAG SECTOR POINTED TO BY CLEARING THE ASSOCIATED ERASE ENABLE REGISTER
(10)
ARE ALL SECTORS VERIFIED?
NO
YES
(11)
END ERASE SEQUENCE BY WITHDRAWING ENABLE ERASE COMMAND

FIG._4

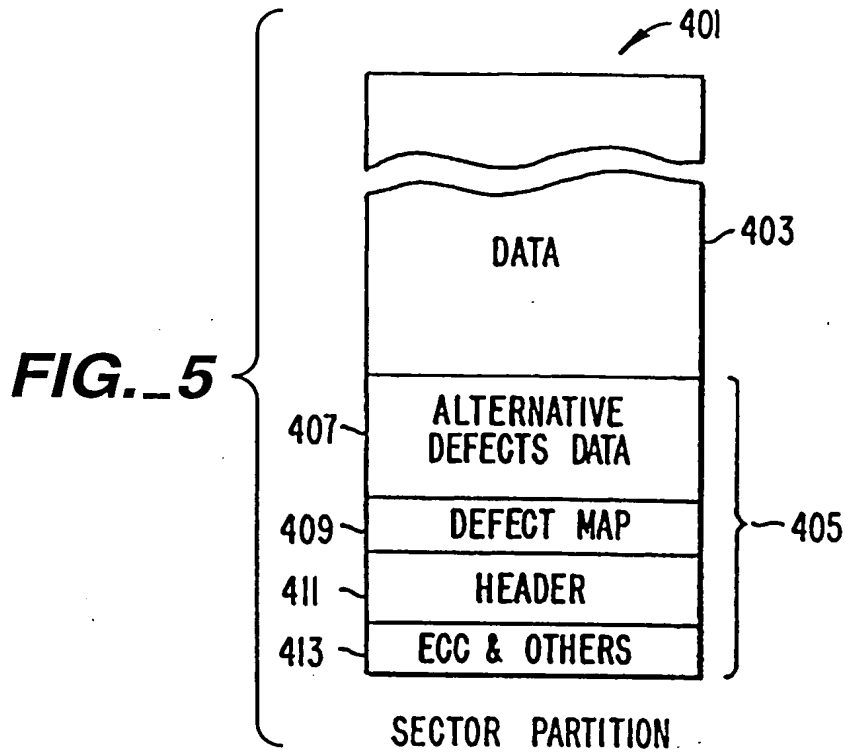

401
DATA
403
ALTERNATIVE DEFECTS DATA
407
DEFECT MAP
409
HEADER
411
ECC & OTHERS
413
405
SECTOR PARTITION

FIG._5

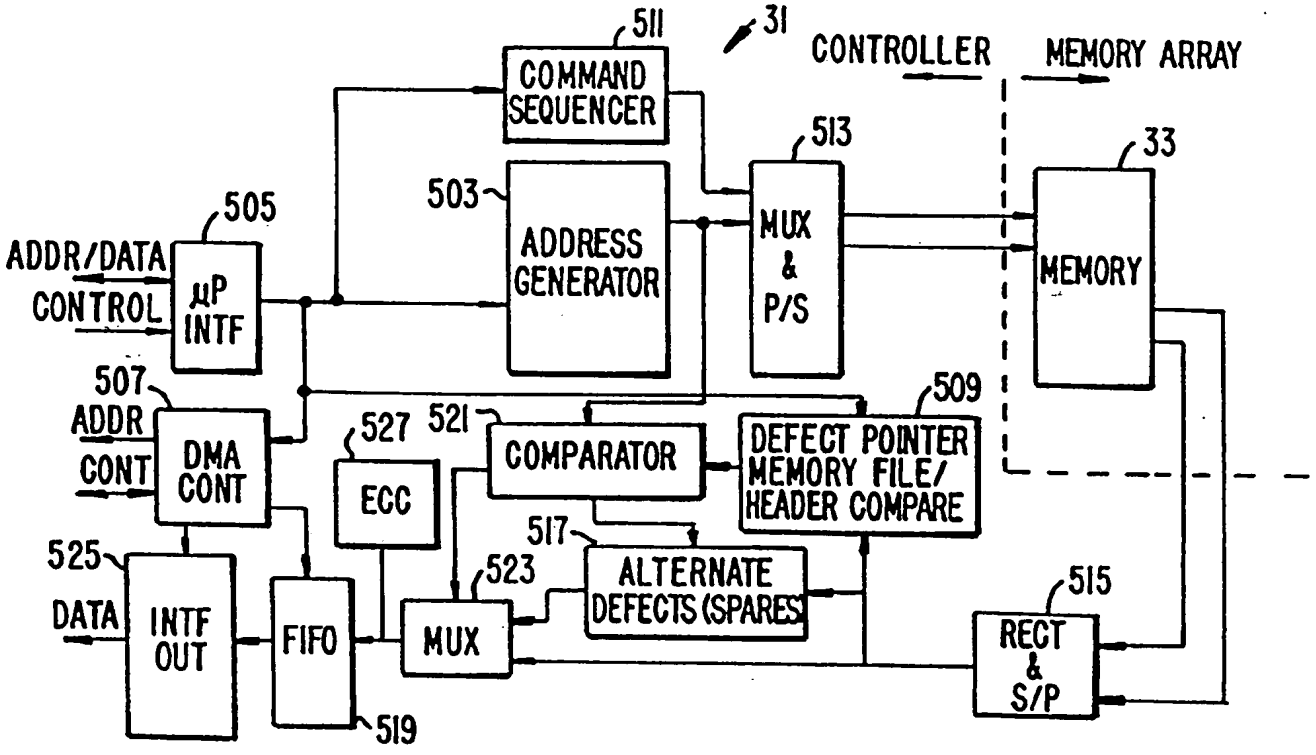

31
CONTROLLER
MEMORY ARRAY
511
COMMAND SEQUENCER
513
33
503
ADDRESS GENERATOR
MUX & P/S
MEMORY
505
ADDR/DATA
CONTROL
µP INTF
507
ADDR
CONT
DMA CONT
509
527
521
ECC
COMPARATOR
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
517
525
523
515
DATA
INTF OUT
FIFO
MUX
ALTERNATE DEFECTS (SPARES)
RECT & S/P
519
READ DATA PATH CONTROL

FIG._6

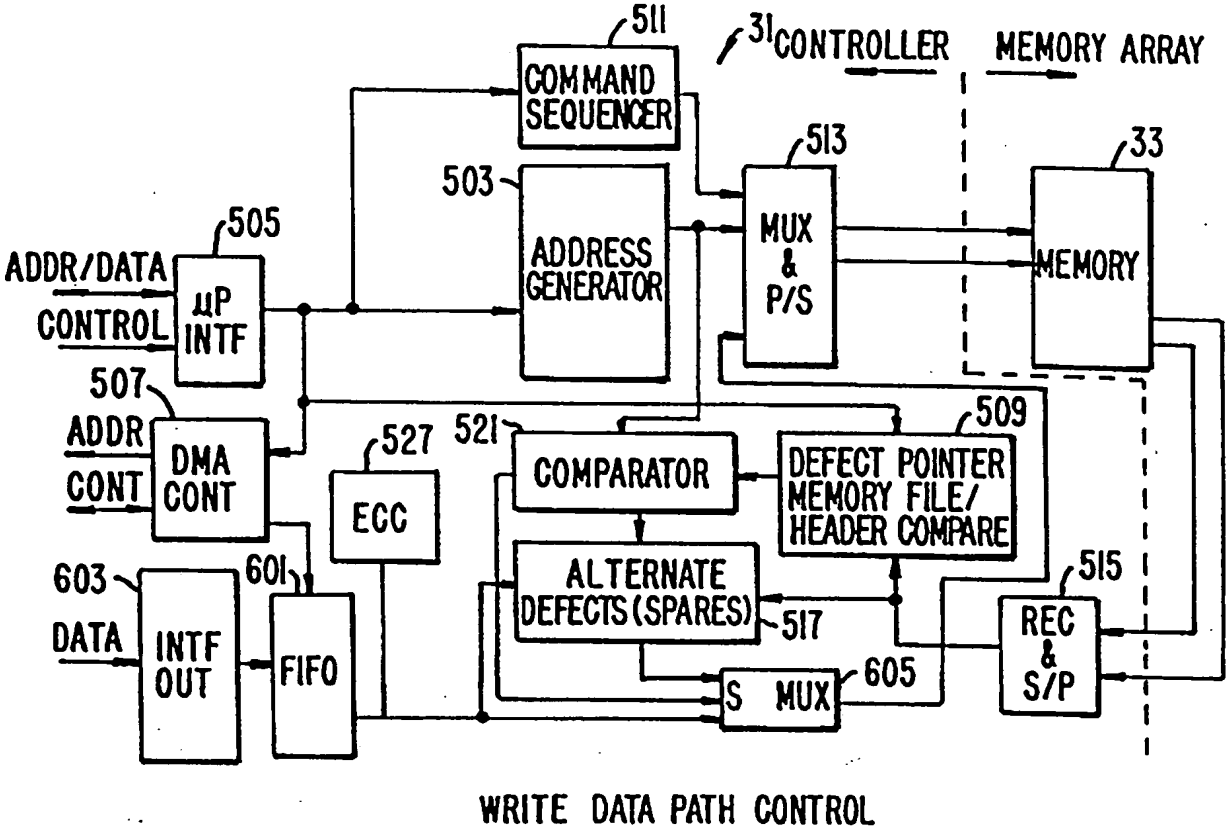

511
31 CONTROLLER
MEMORY ARRAY
COMMAND SEQUENCER
513
33
503
505
ADDR/DATA
CONTROL
μP INTF
ADDRESS GENERATOR
MUX & P/S
MEMORY
507
ADDR
CONT
DMA CONT
527
521
509
ECC
COMPARATOR
DEFECT POINTER MEMORY FILE/ HEADER COMPARE
603
601
515
DATA
INTF OUT
FIFO
ALTERNATE DEFECTS (SPARES)
517
REC & S/P
S MUX
605
WRITE DATA PATH CONTROL

FIG._7

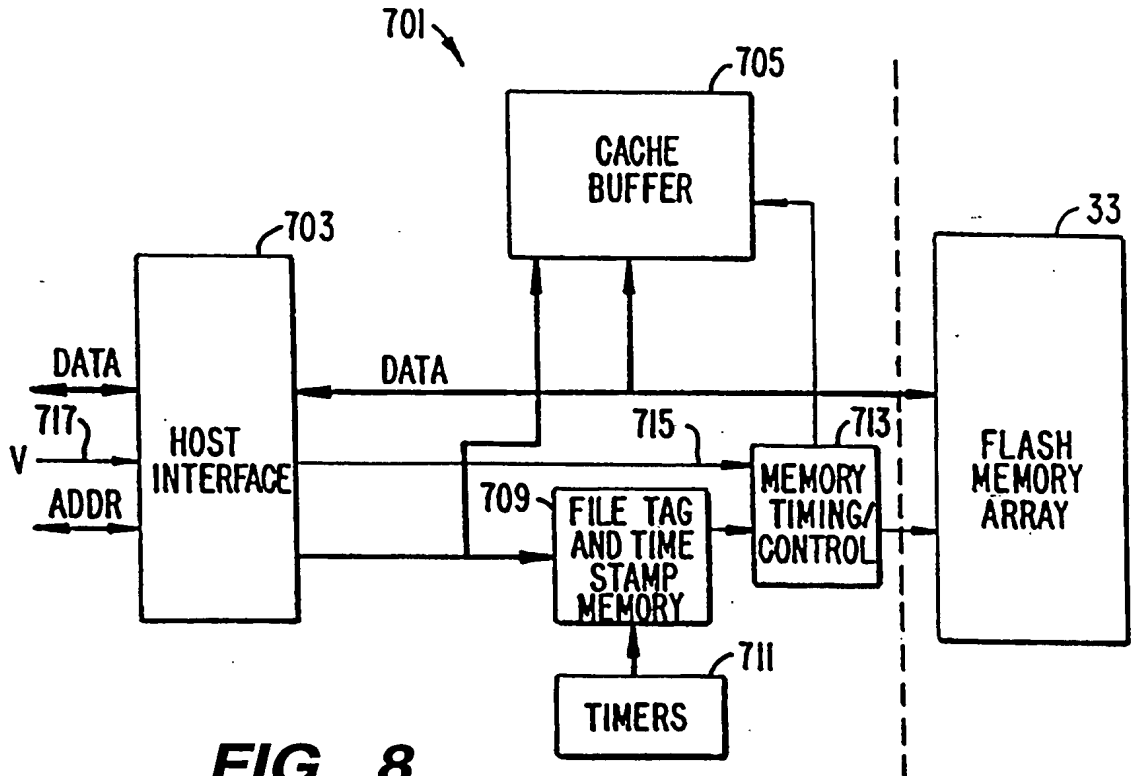

701
705
CACHE BUFFER
703
33
DATA
DATA
717
V
715
713
HOST INTERFACE
FLASH MEMORY ARRAY
ADDR
709
FILE TAG AND TIME STAMP MEMORY
MEMORY TIMING/ CONTROL
711
TIMERS

FIG._8

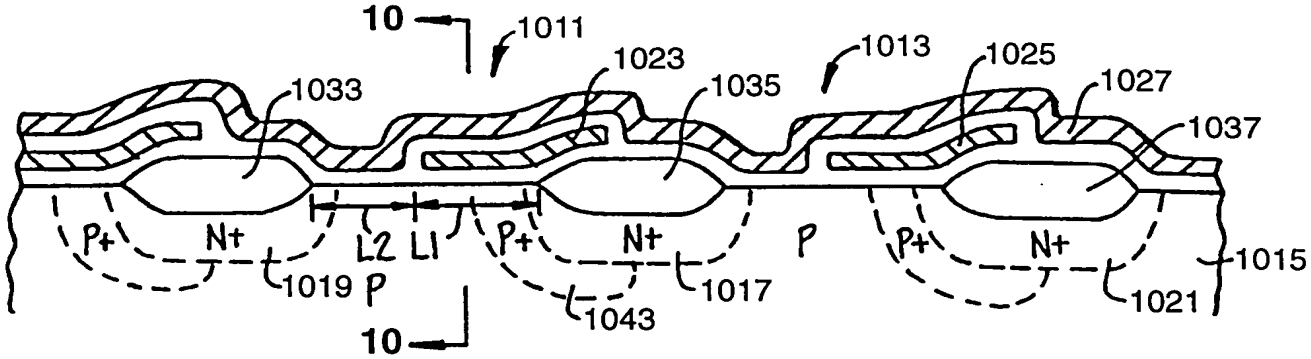


FIG._9

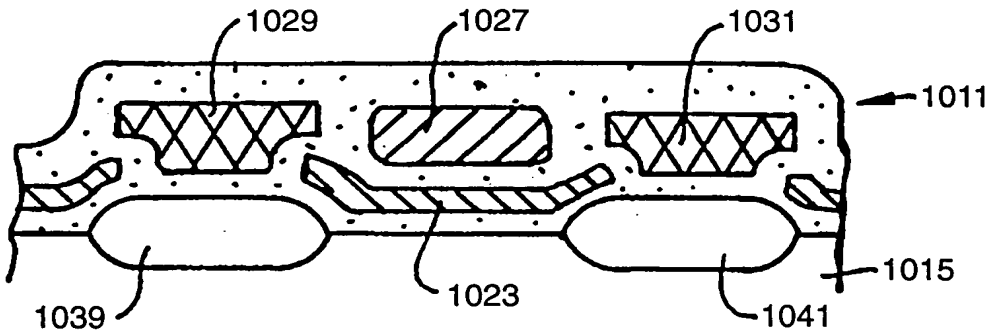


FIG._10

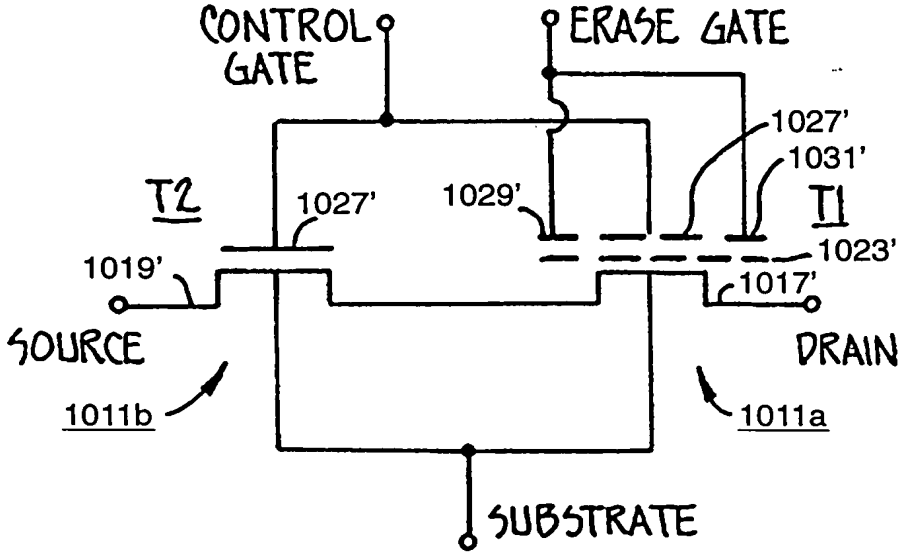


FIG._11

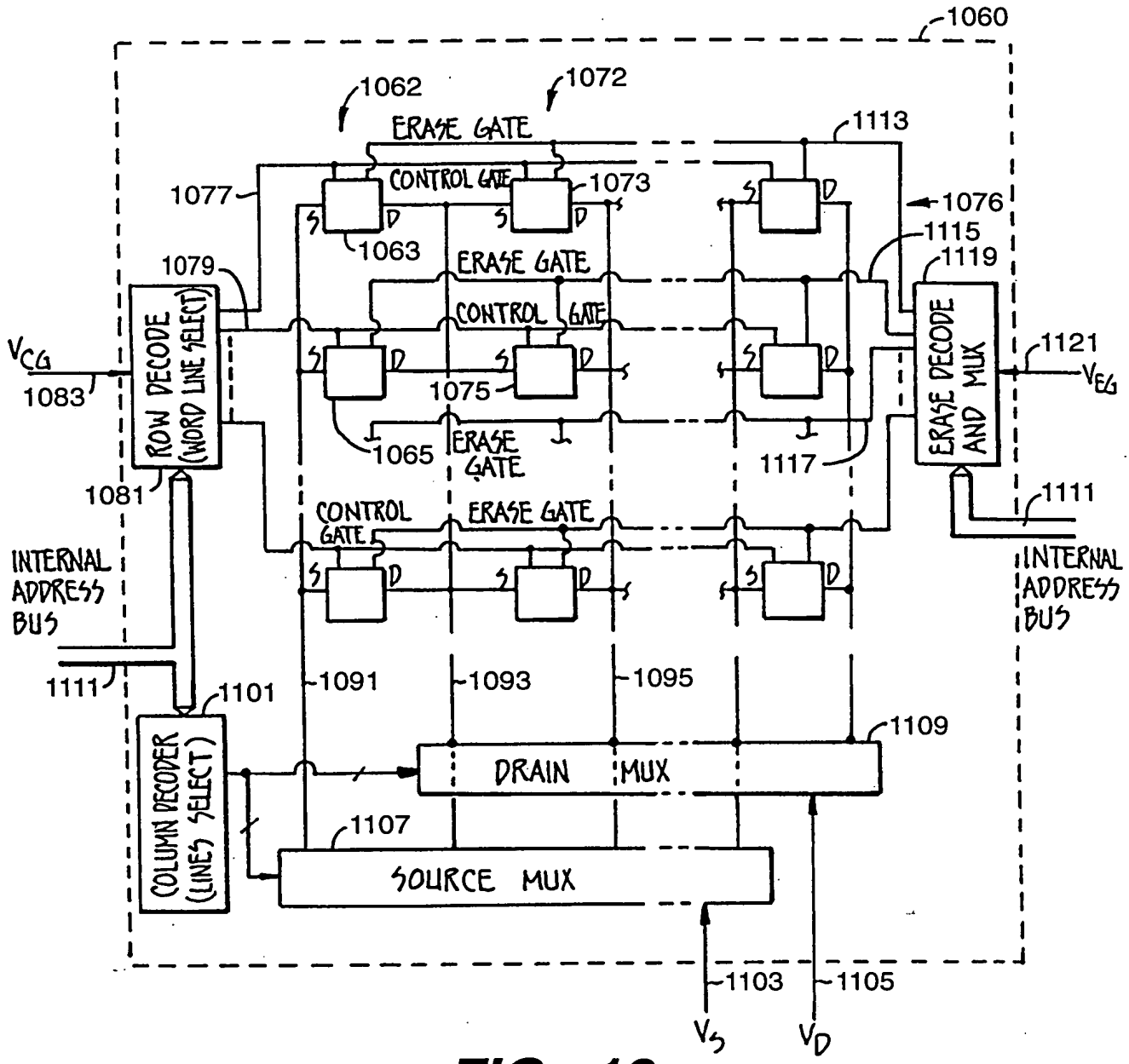

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
1115
1119
ERASE GATE
1079
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
ERASE DECODE AND MUX
1121
V_{CG}
1083
1075
V_{EG}
1065
ERASE GATE
1117
1081
CONTROL GATE
ERASE GATE
1111
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
COLUMN DECODER (LINES SELECT)
DRAIN MUX
1107
SOURCE MUX
1103
1105
V_S
V_D

FIG._12

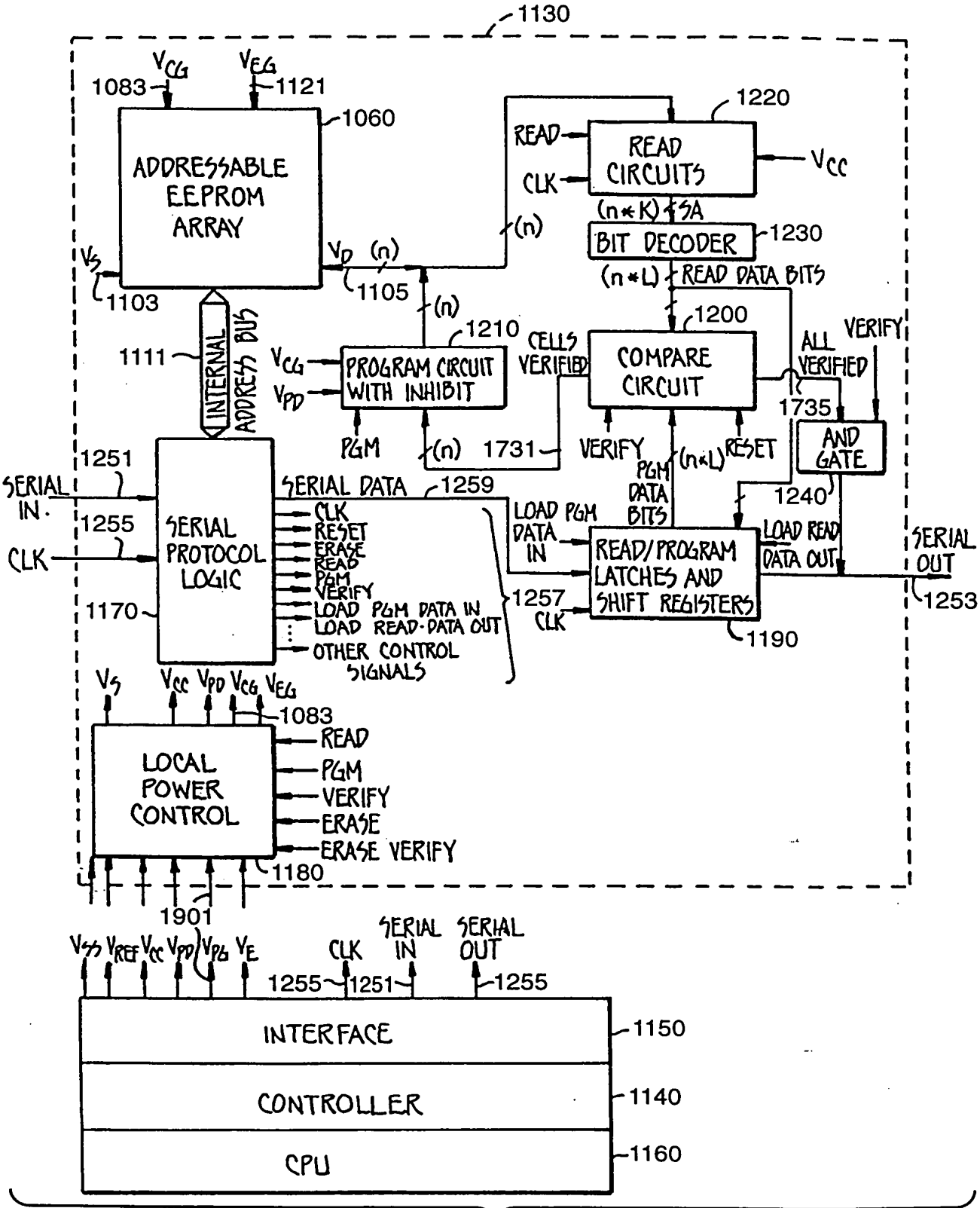

1130
ADDRESSABLE EEPROM ARRAY
1060
1083
1121
1103
1105
INTERNAL ADDRESS BUS
1111
PROGRAM CIRCUIT WITH INHIBIT
1210
READ CIRCUITS
1220
BIT DECODER
1230
COMPARE CIRCUIT
1200
AND GATE
1240
1735
SERIAL PROTOCOL LOGIC
1170
1251
1255
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ-DATA OUT
OTHER CONTROL SIGNALS
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1257
1190
LOCAL POWER CONTROL
1180
1901
INTERFACE
1150
CONTROLLER
1140
CPU
1160
SERIAL IN
SERIAL OUT
1253

FIG._13

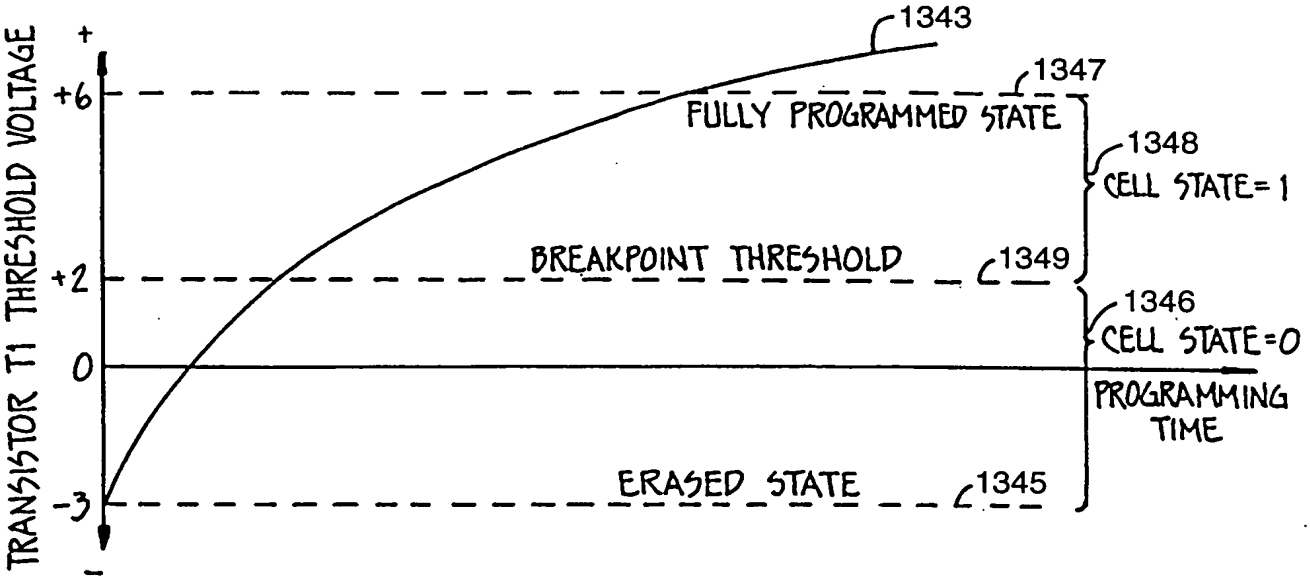


FIG._14

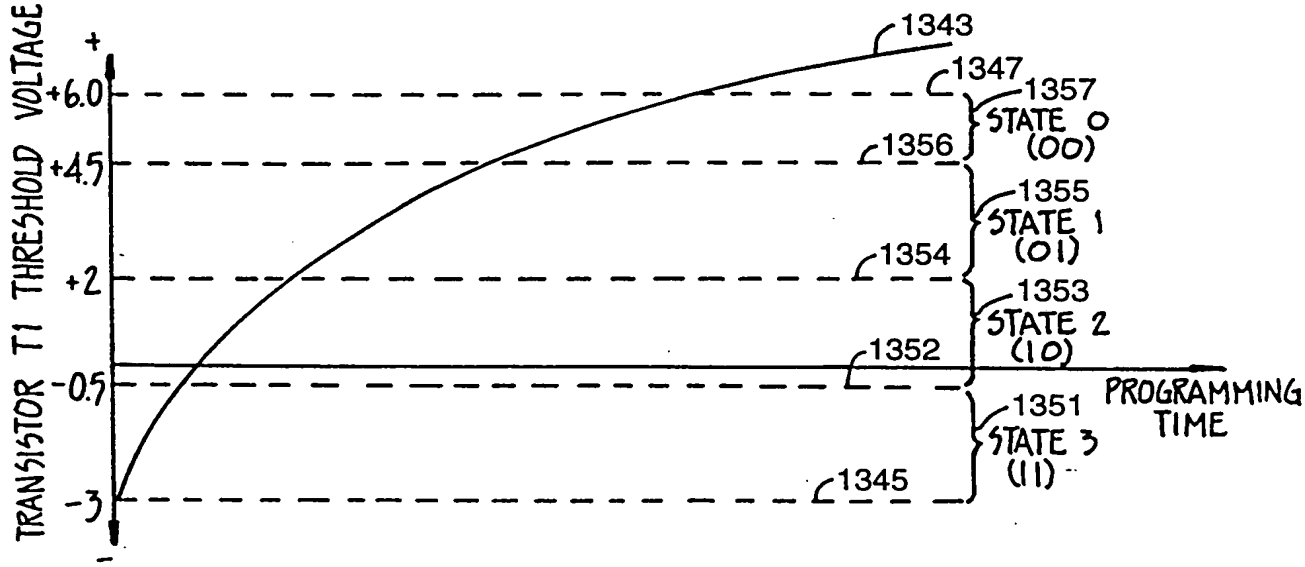


FIG._15A

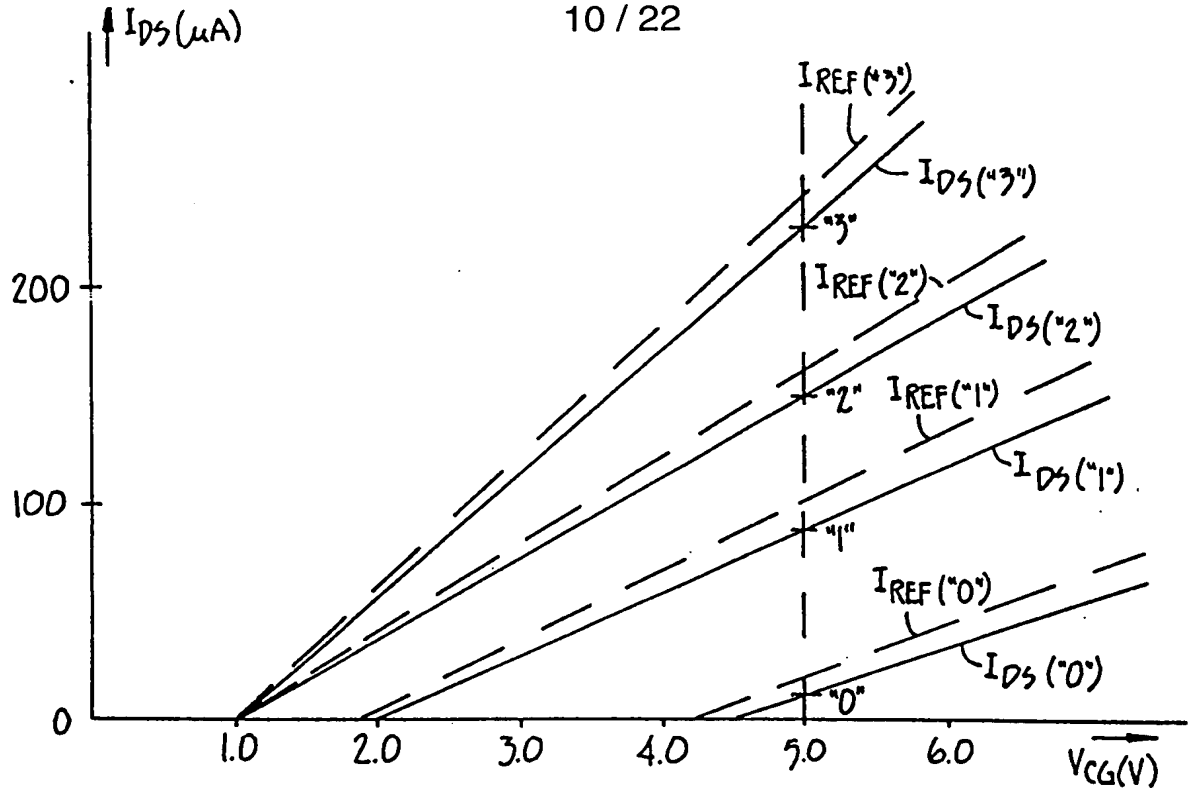


FIG._15B

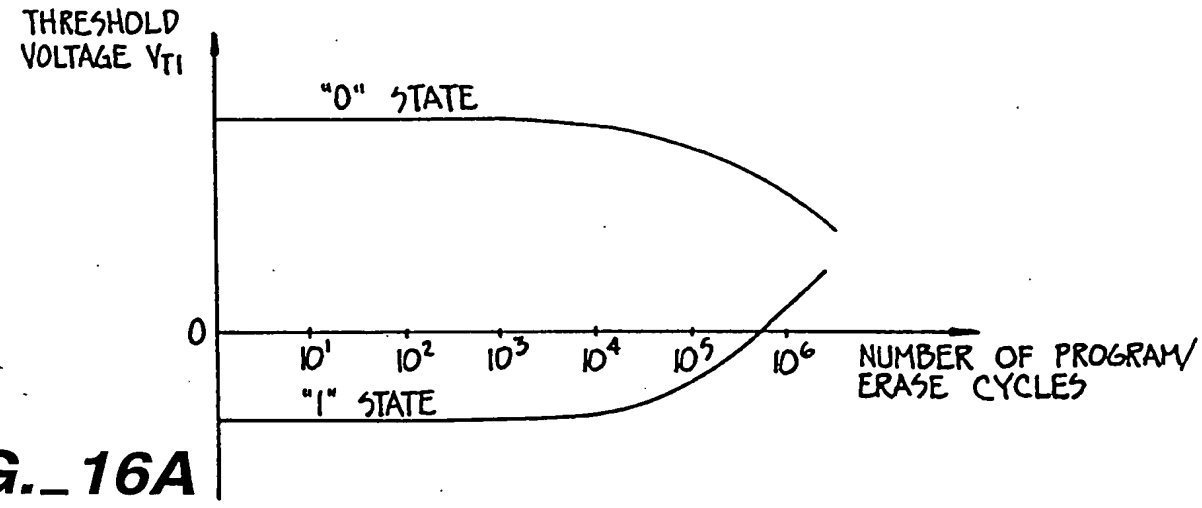


FIG._16A

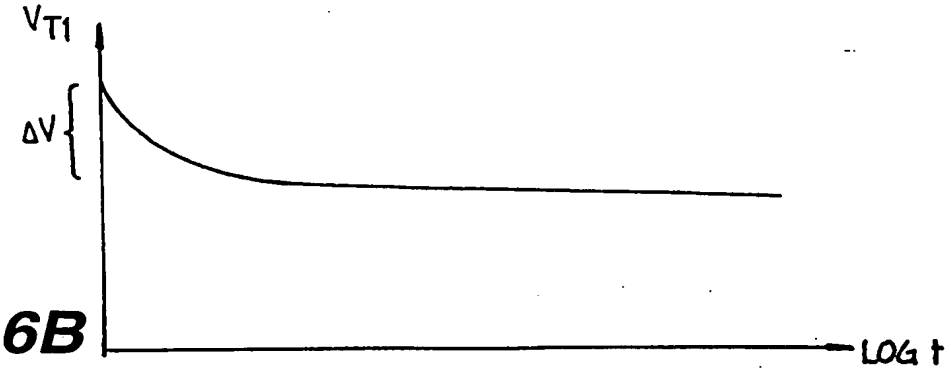


FIG._16B

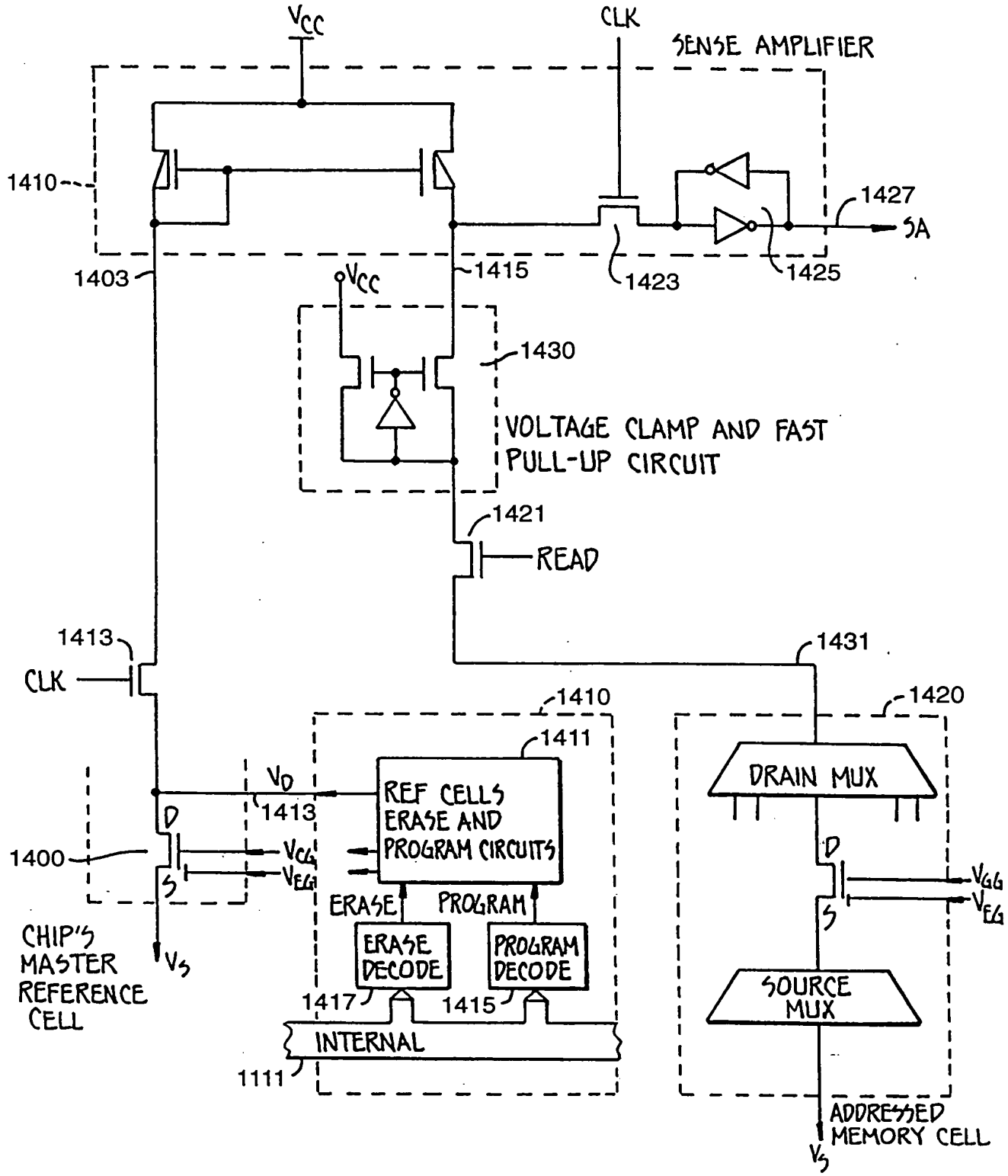

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{GG}
V_{EG}
S
ERASE
PROGRAM
CHIP'S MASTER REFERENCE CELL
V_S
ERASE DECODE
PROGRAM DECODE
SOURCE MUX
1417
1415
INTERNAL
1111
ADDRESSED MEMORY CELL
V_S

FIG._17A

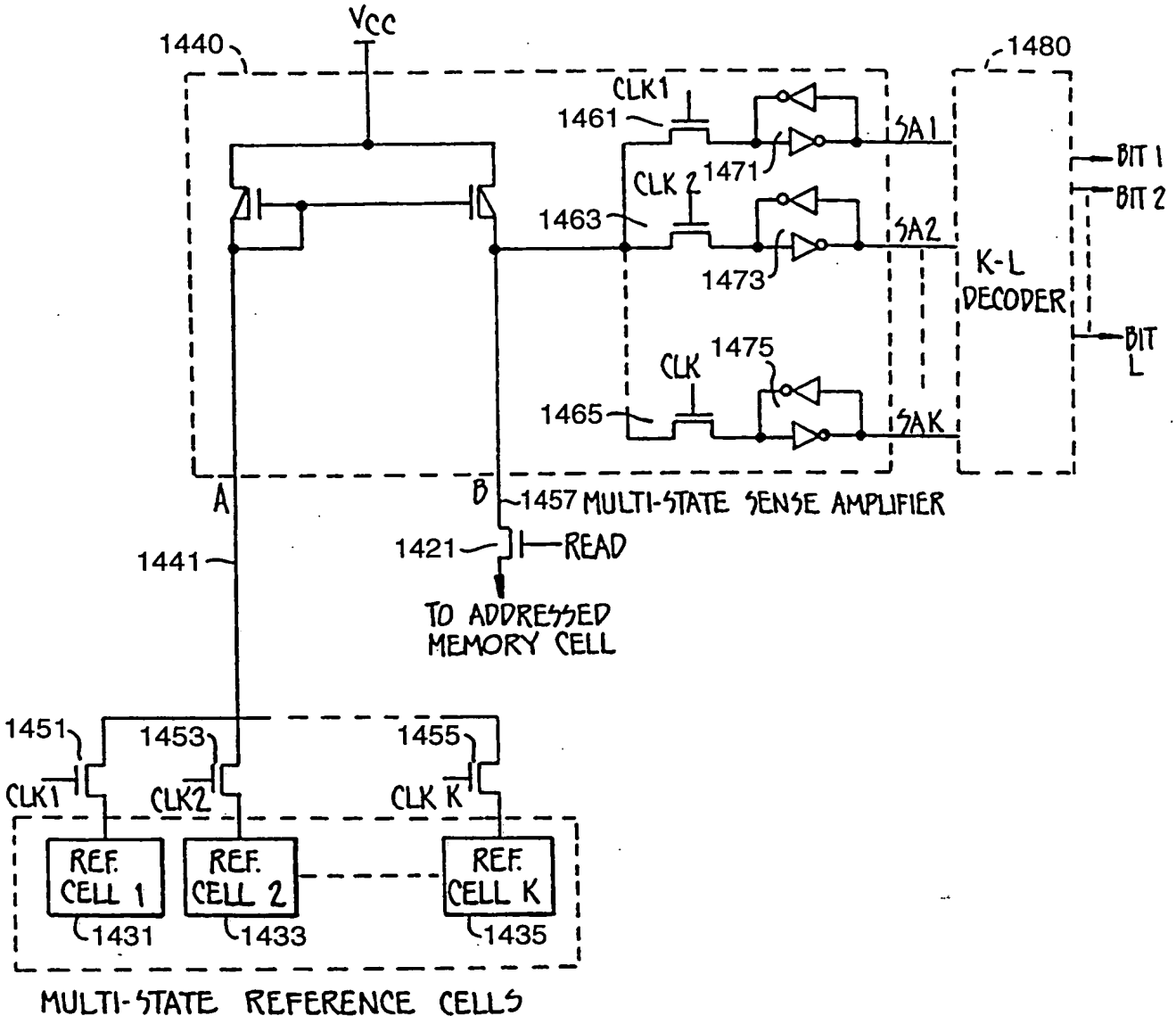

Vcc
1440
1480
CLK1
1461
SA1
1471
BIT 1
BIT 2
CLK 2
1463
SA2
1473
K-L
DECODER
CLK
1475
BIT
L
1465
SAK
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1421
READ
1441
TO ADDRESSED
MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG._17B

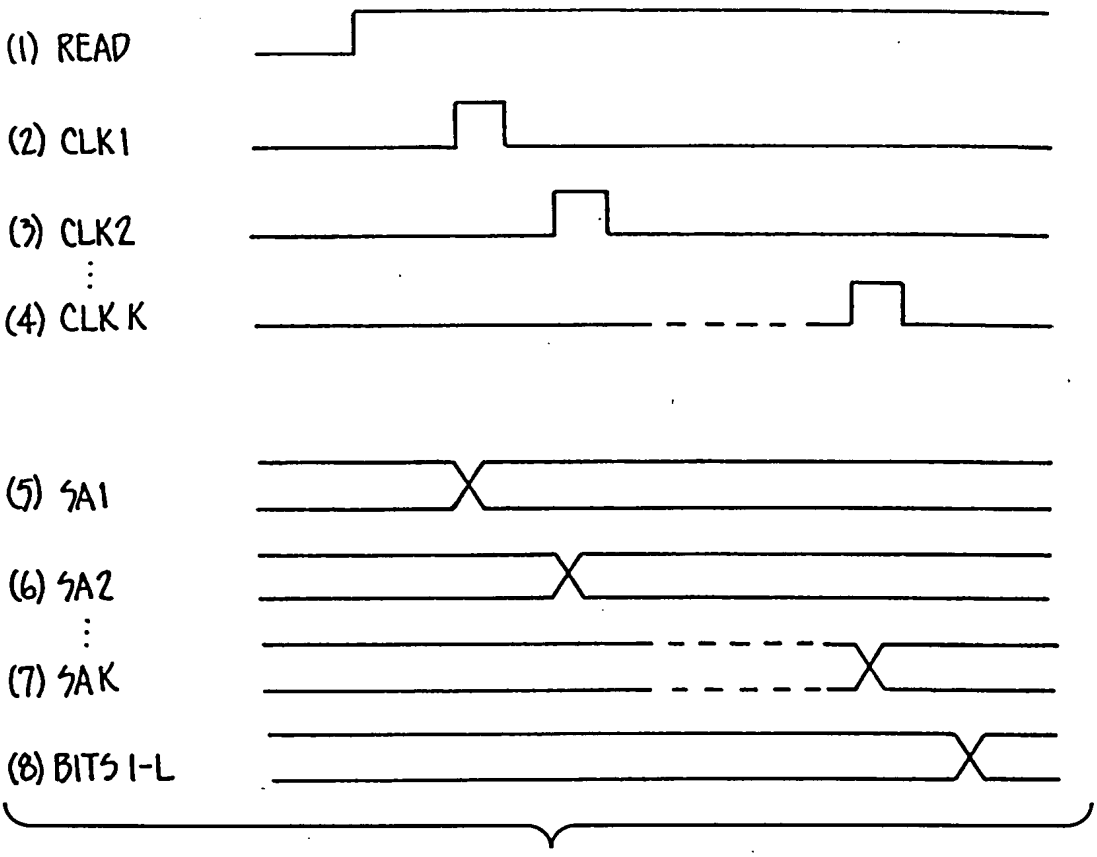


FIG._17C

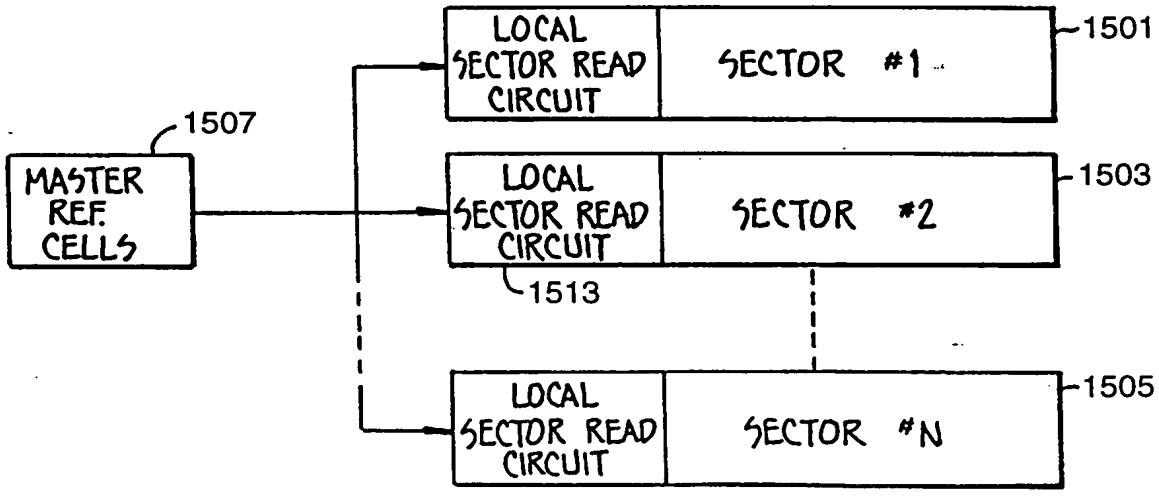


FIG._18

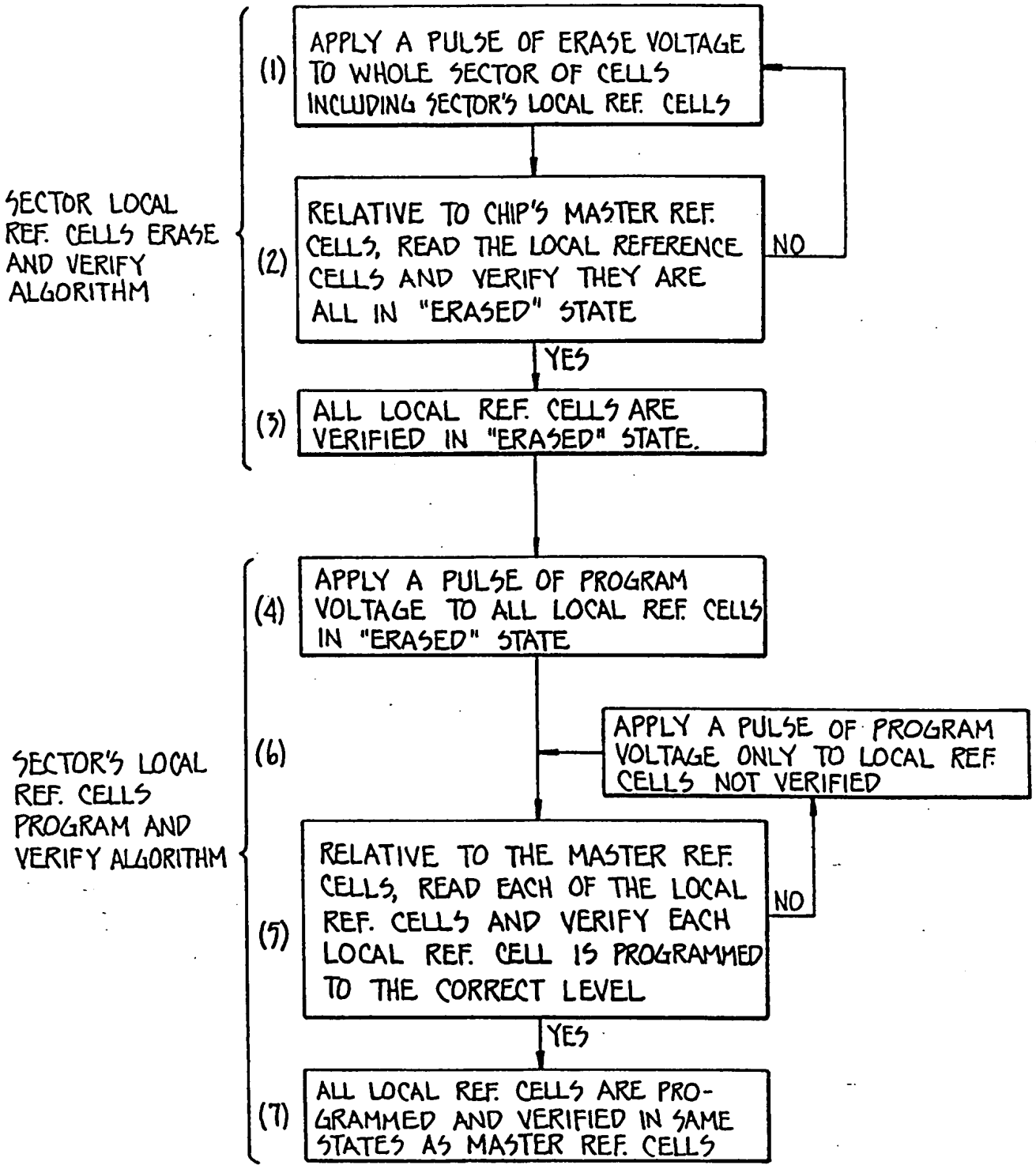

SECTOR LOCAL REF. CELLS ERASE AND VERIFY ALGORITHM
(1) APPLY A PULSE OF ERASE VOLTAGE TO WHOLE SECTOR OF CELLS INCLUDING SECTOR'S LOCAL REF. CELLS
(2) RELATIVE TO CHIP'S MASTER REF. CELLS, READ THE LOCAL REFERENCE CELLS AND VERIFY THEY ARE ALL IN "ERASED" STATE
NO
YES
(3) ALL LOCAL REF. CELLS ARE VERIFIED IN "ERASED" STATE.
SECTOR'S LOCAL REF. CELLS PROGRAM AND VERIFY ALGORITHM
(4) APPLY A PULSE OF PROGRAM VOLTAGE TO ALL LOCAL REF. CELLS IN "ERASED" STATE
(6) APPLY A PULSE OF PROGRAM VOLTAGE ONLY TO LOCAL REF. CELLS NOT VERIFIED
(5) RELATIVE TO THE MASTER REF. CELLS, READ EACH OF THE LOCAL REF. CELLS AND VERIFY EACH LOCAL REF. CELL IS PROGRAMMED TO THE CORRECT LEVEL
NO
YES
(7) ALL LOCAL REF. CELLS ARE PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

FIG._19

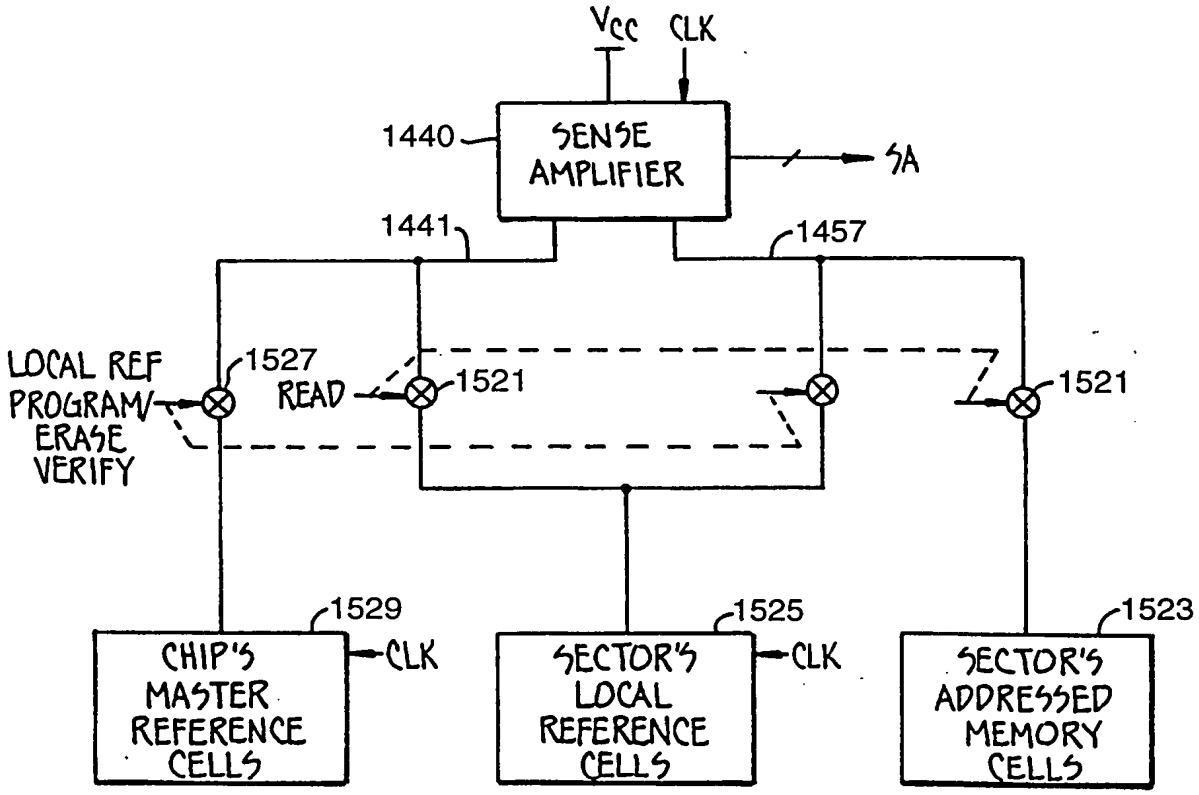


FIG._20A

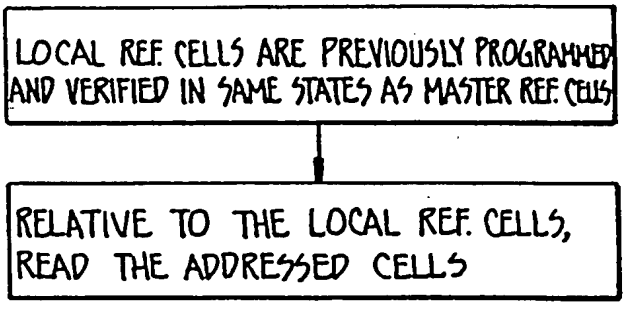
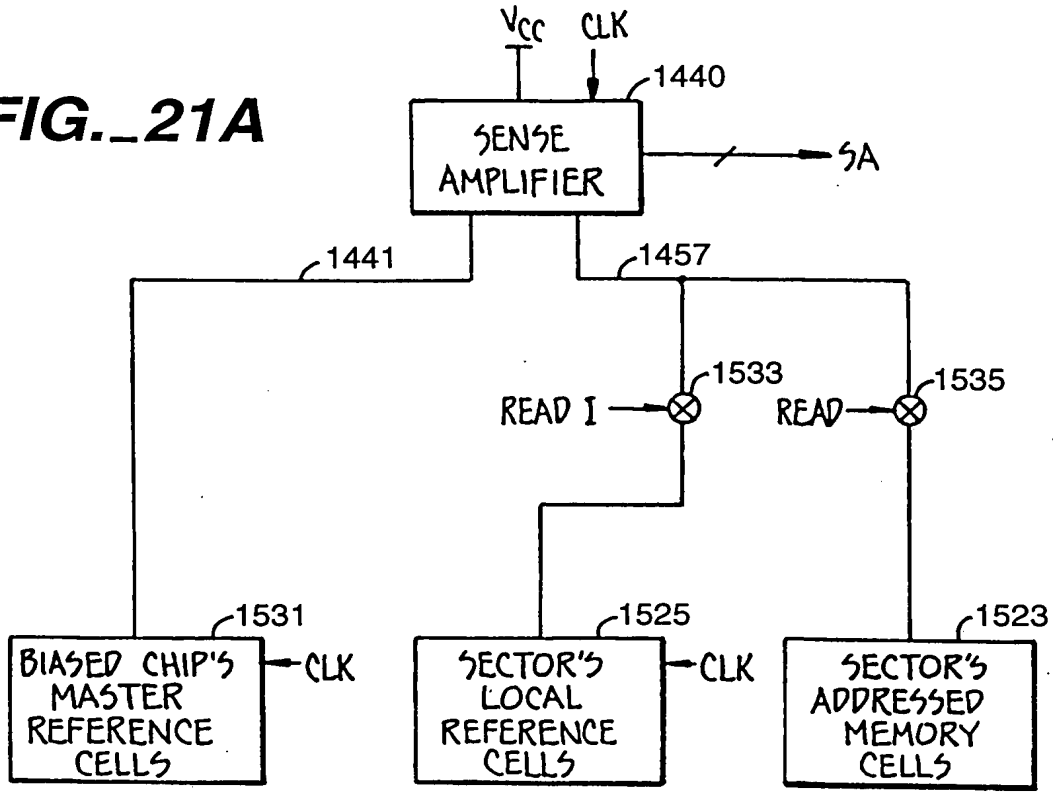


FIG._20B

FIG._21A



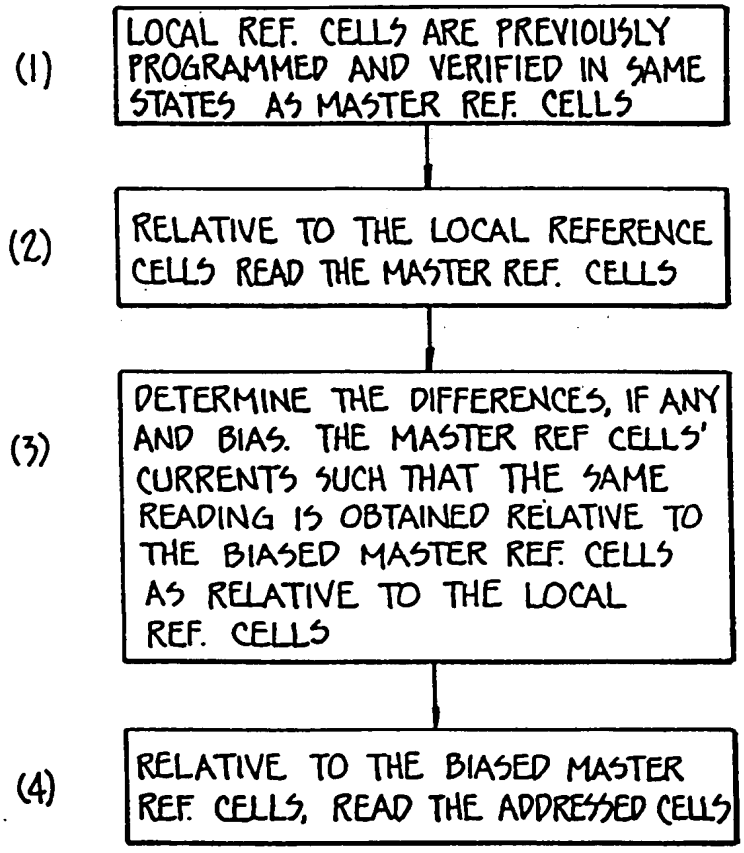


FIG._21D

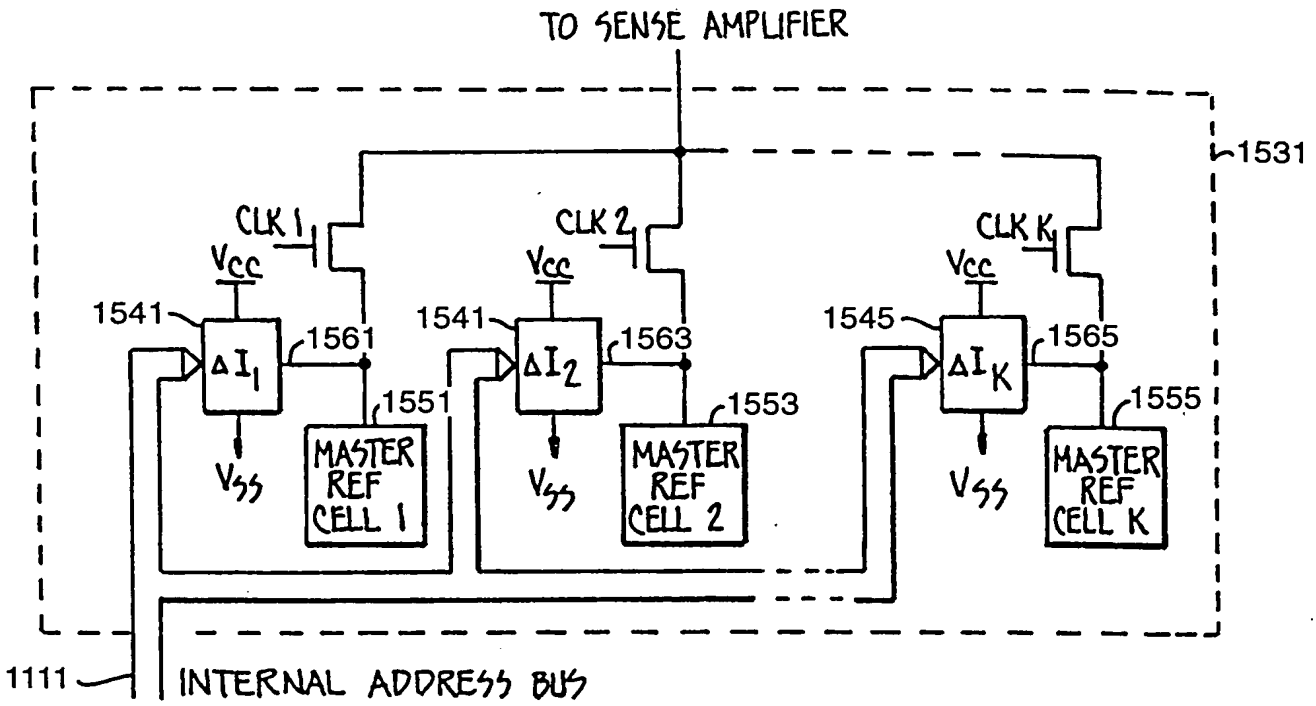


FIG._21B

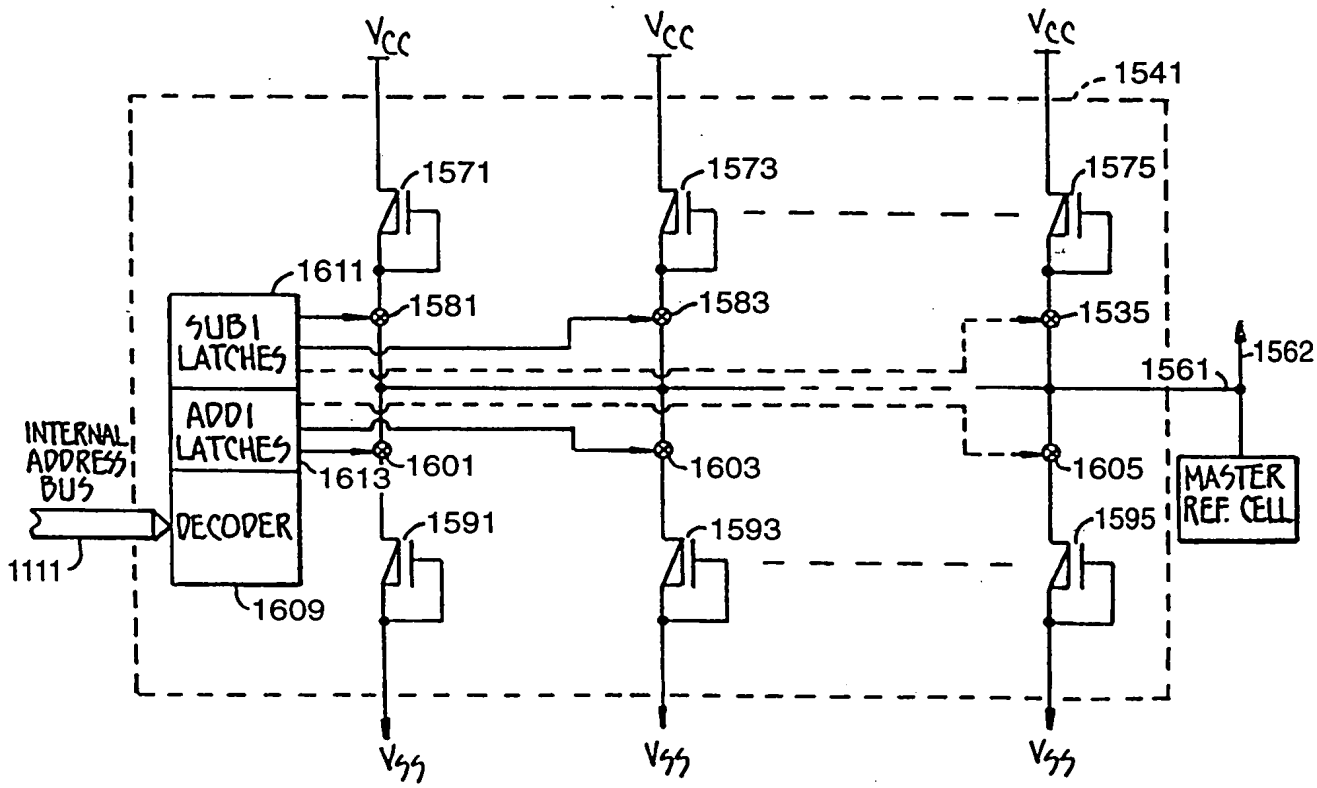
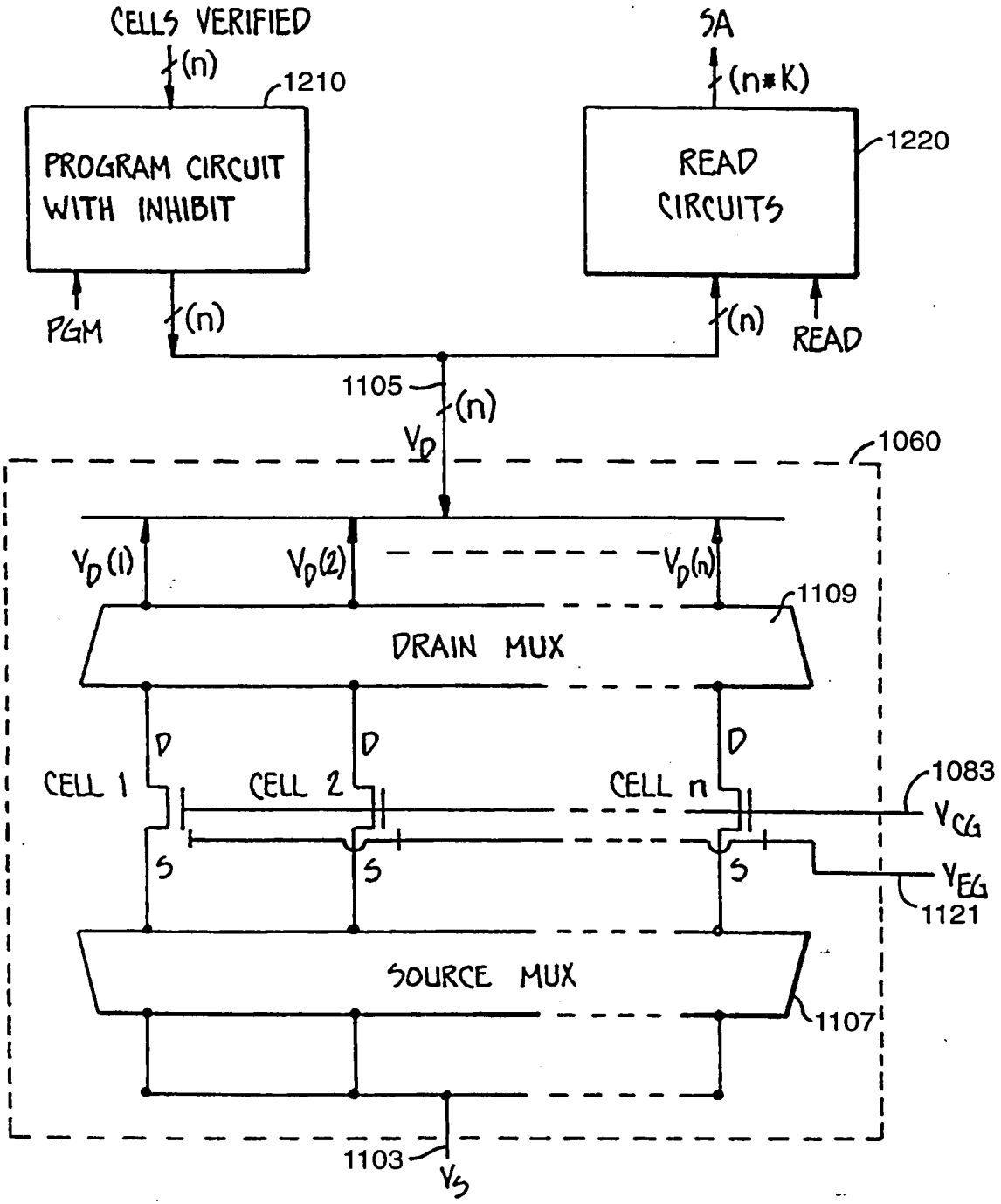
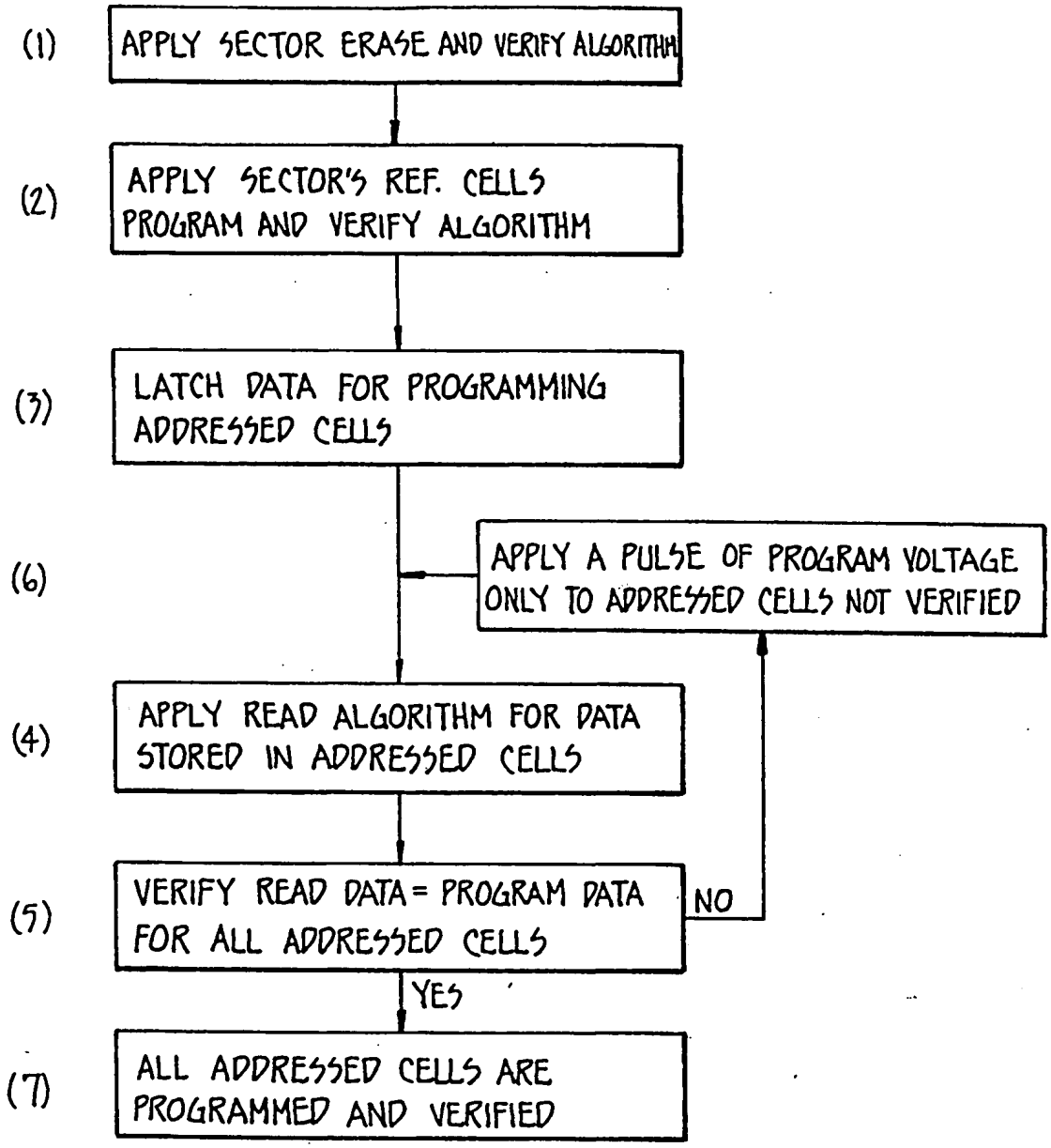


FIG._21C



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22



PROGRAM ALGORITHM

FIG._23

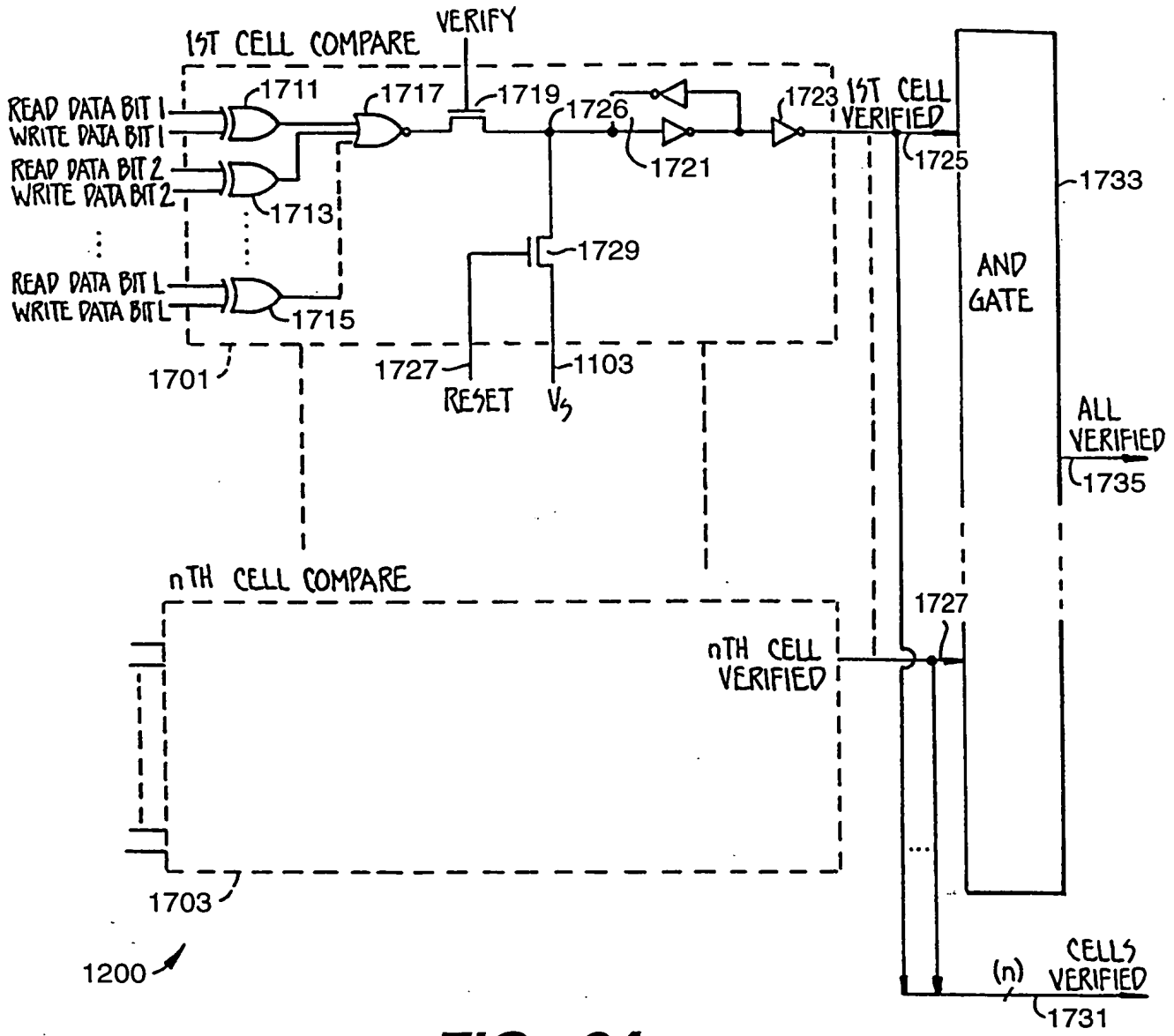

1ST CELL COMPARE
VERIFY
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
1711
1717
1719
1726
1723
1721
1713
1715
1729
1701
1727
RESET
1103
1ST CELL VERIFIED
1725
1733
AND GATE
ALL VERIFIED
1735
nTH CELL COMPARE
nTH CELL VERIFIED
1727
1703
1200
(n) CELLS VERIFIED
1731

FIG._24

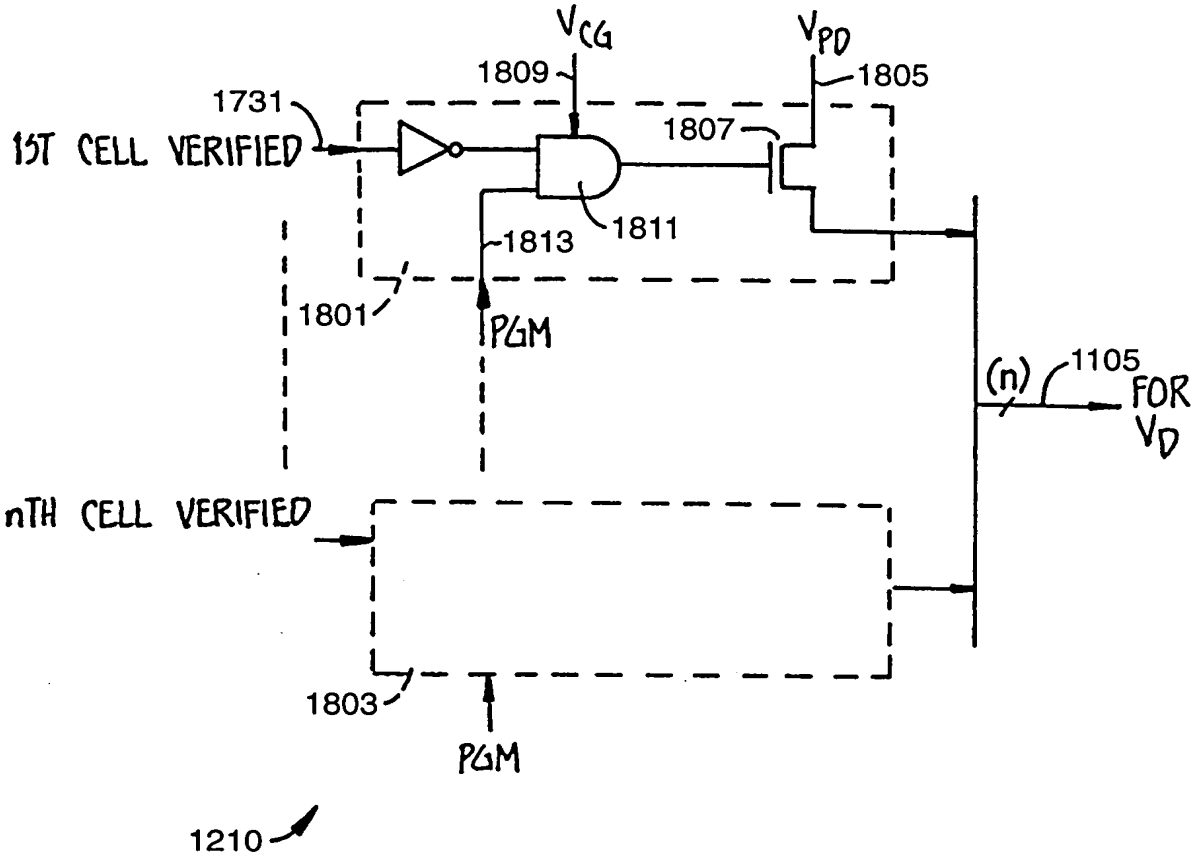

V_{CG}
V_{PD}
1809
1805
1731
1807
1ST CELL VERIFIED
1811
1813
1801
PGM
(n)
1105
FOR V_D
nTH CELL VERIFIED
1803
PGM
1210

FIG._25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

TABLE 1

FIG._26

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

TABLE 2

FIG._27

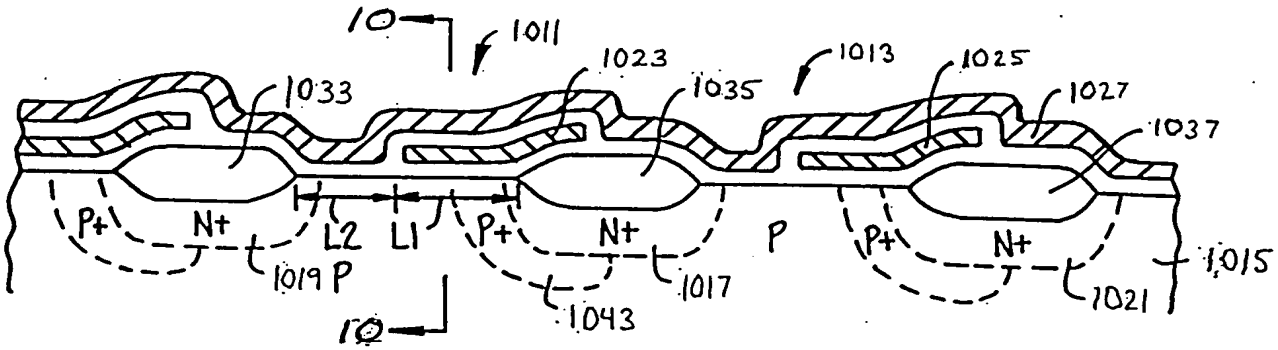


FIG. 9

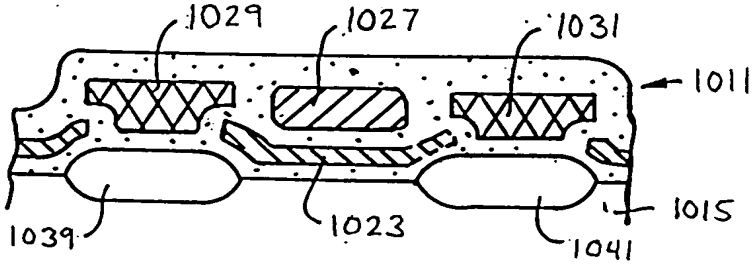


FIG. 10

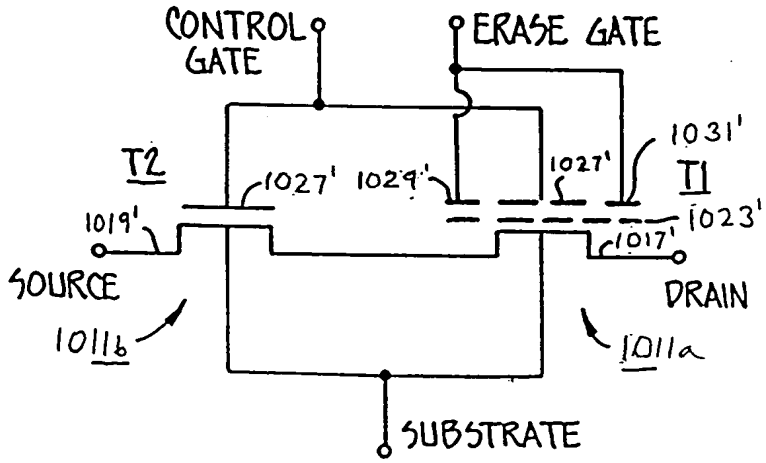


FIG. 11

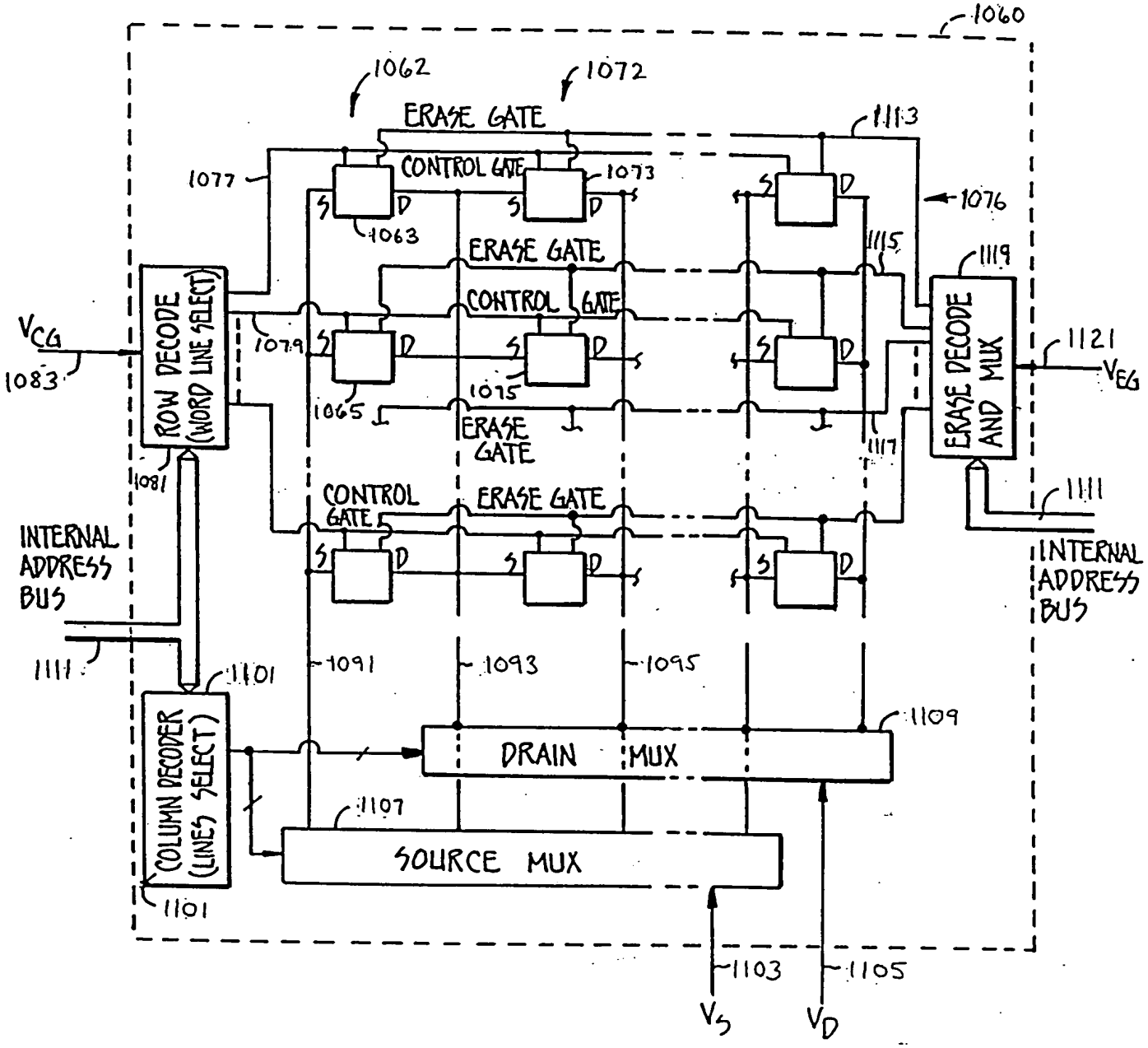

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
ERASE GATE
1115
1119
CONTROL GATE
V_{CG}
1083
ROW DECODE (WORD LINE SELECT)
1079
1121
V_{EG}
ERASE DECODE AND MUX
1065
1075
ERASE GATE
1117
1081
CONTROL GATE
ERASE GATE
1111
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
COLUMN DECODER (LINES SELECT)
DRAIN MUX
1107
SOURCE MUX
1101
1103
1105
V_S
V_D

FIG. 12.

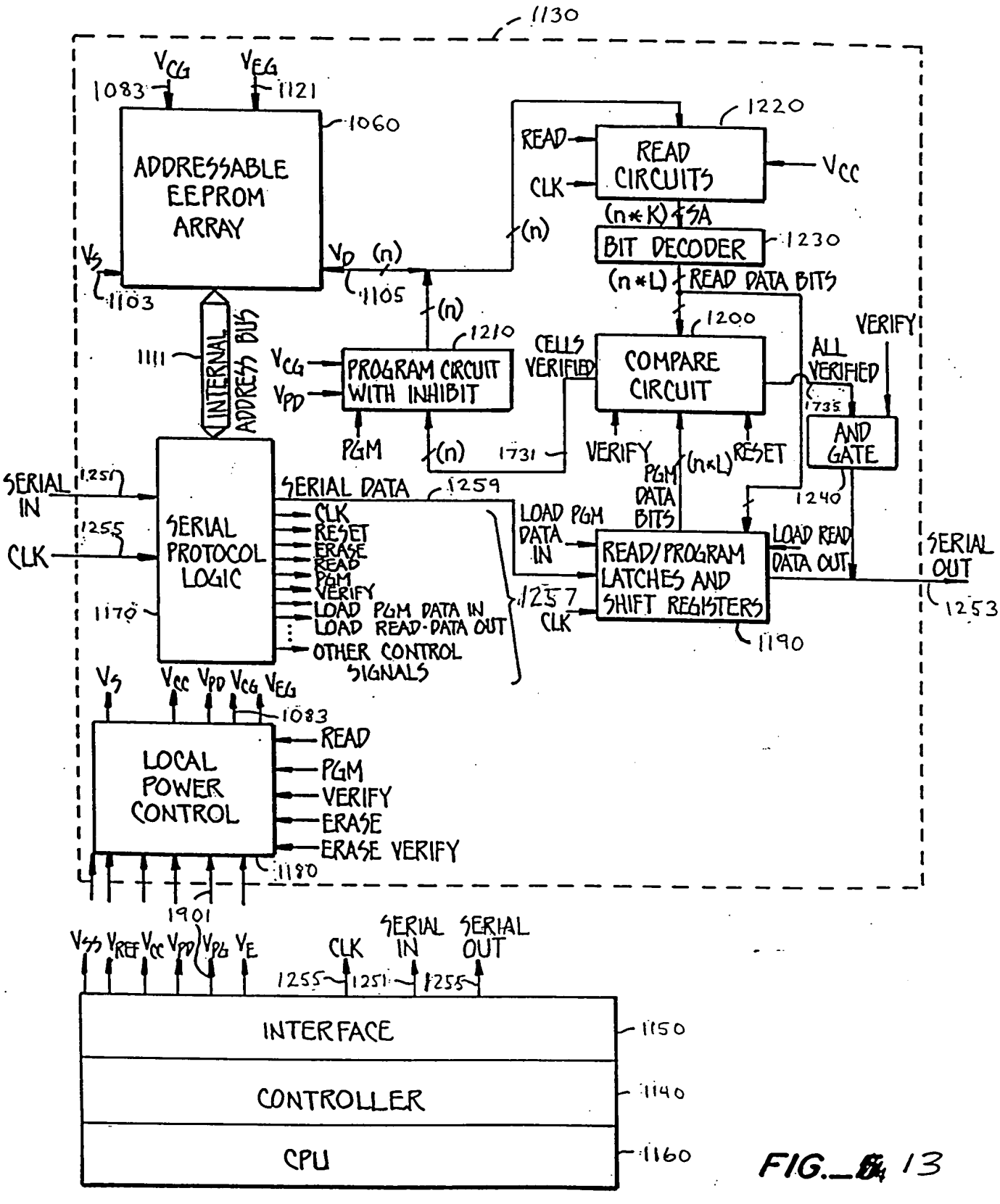

1130
V_{CG}
V_{EG}
1083
1121
ADDRESSABLE EEPROM ARRAY
1060
V_S
1103
V_D (n)
1105
INTERNAL ADDRESS BUS
1111
(n)
1210
V_{CG}
V_{PD}
PROGRAM CIRCUIT WITH INHIBIT
PGM
(n)
1220
READ
CLK
READ CIRCUITS
V_{CC}
(n*K) SA
BIT DECODER
1230
(n*L) READ DATA BITS
1200
CELLS VERIFIED
COMPARE CIRCUIT
1731
VERIFY
(n*L)
RESET
ALL VERIFIED
1735
VERIFY
AND GATE
1240
SERIAL IN
1251
1255
CLK
SERIAL PROTOCOL LOGIC
1170
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ-DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
PGM DATA BITS
1257
CLK
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1190
LOAD READ DATA OUT
SERIAL OUT
1253
V_S
V_{CC}
V_{PD}
V_{CG}
V_{EG}
1083
LOCAL POWER CONTROL
READ
PGM
VERIFY
ERASE
ERASE VERIFY
1180
1901
V_{SS}
V_{REF}
V_{CC}
V_{PD}
V_{PG}
V_E
CLK
SERIAL IN
SERIAL OUT
1255
1251
1255
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG. 13

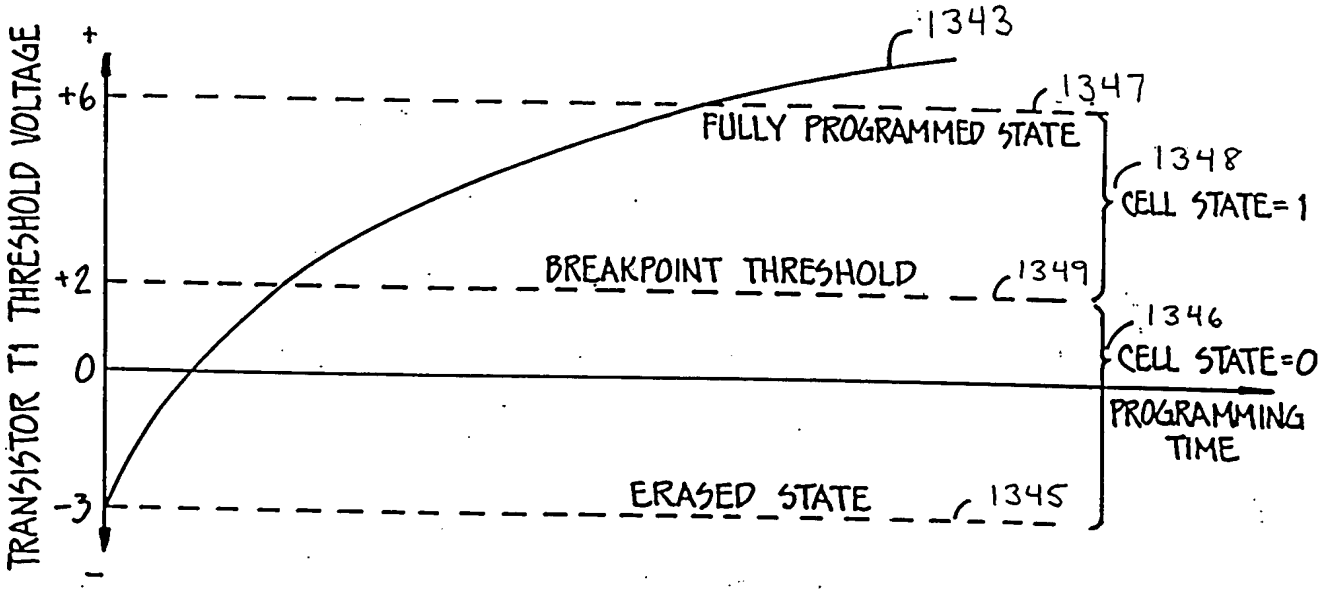


FIG. 14.

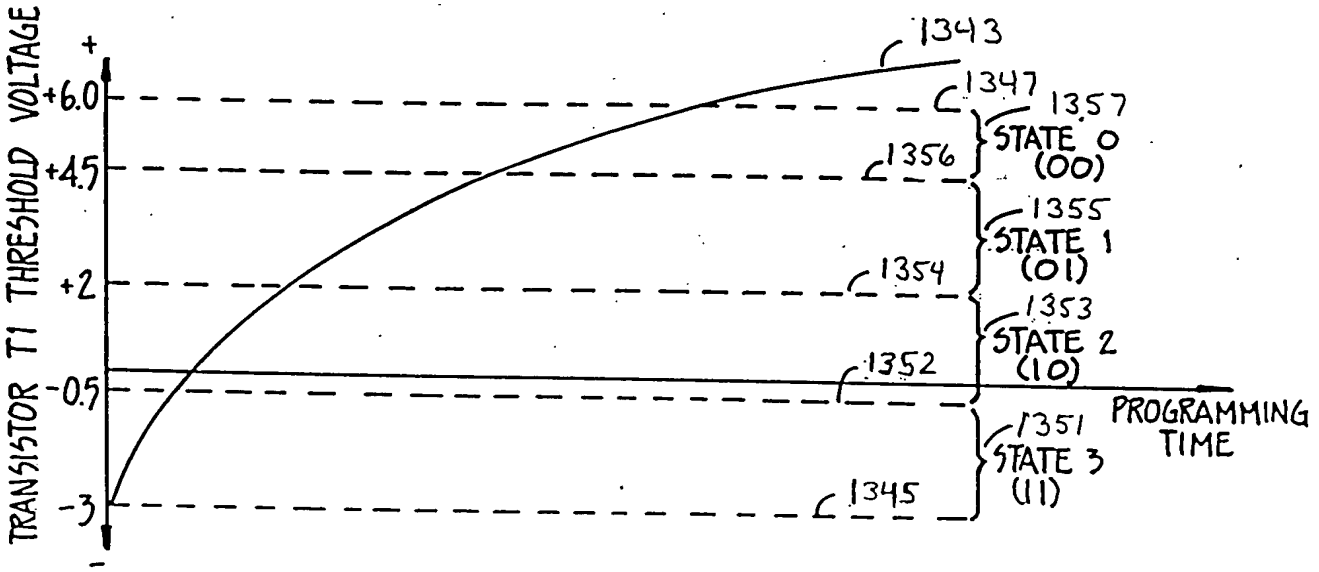


FIG. 15A

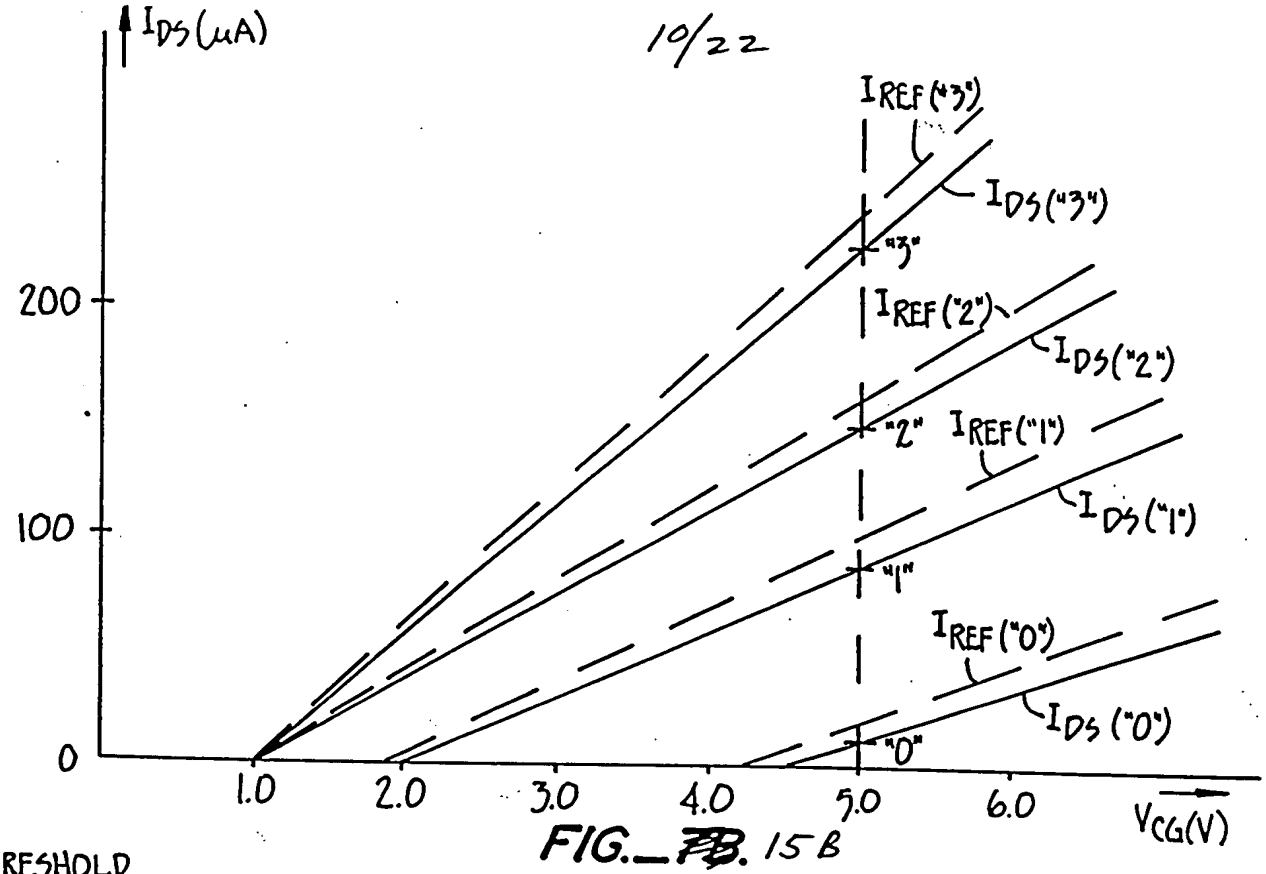


FIG. 15B

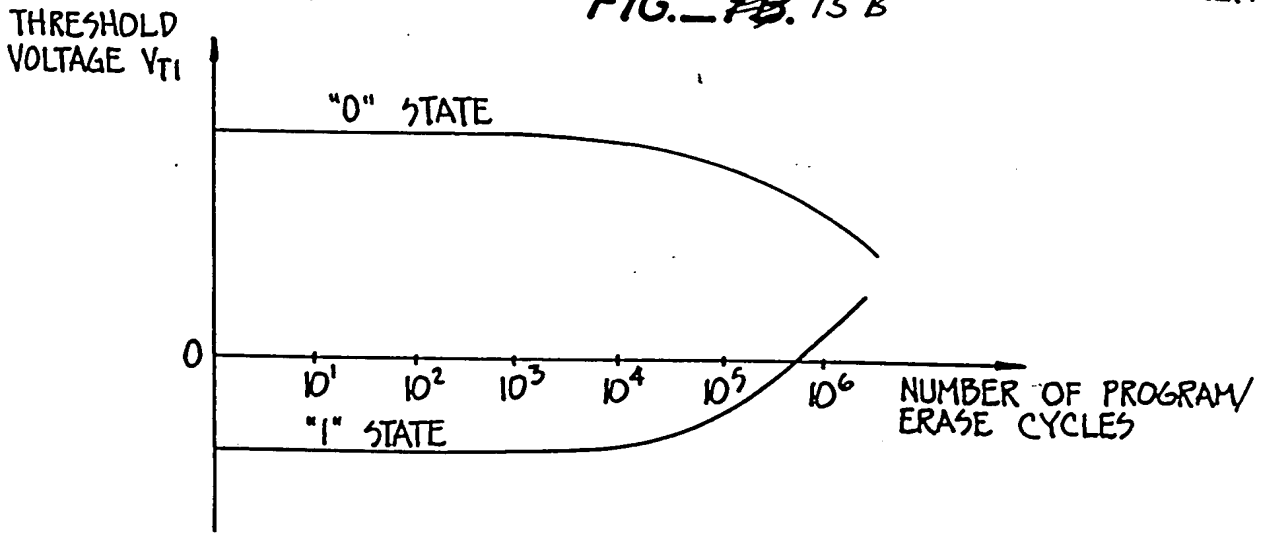


FIG. 16A

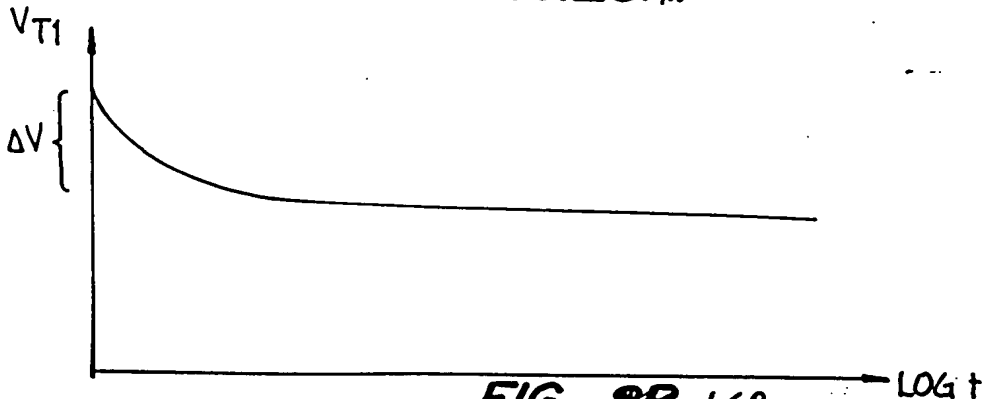


FIG. 16B

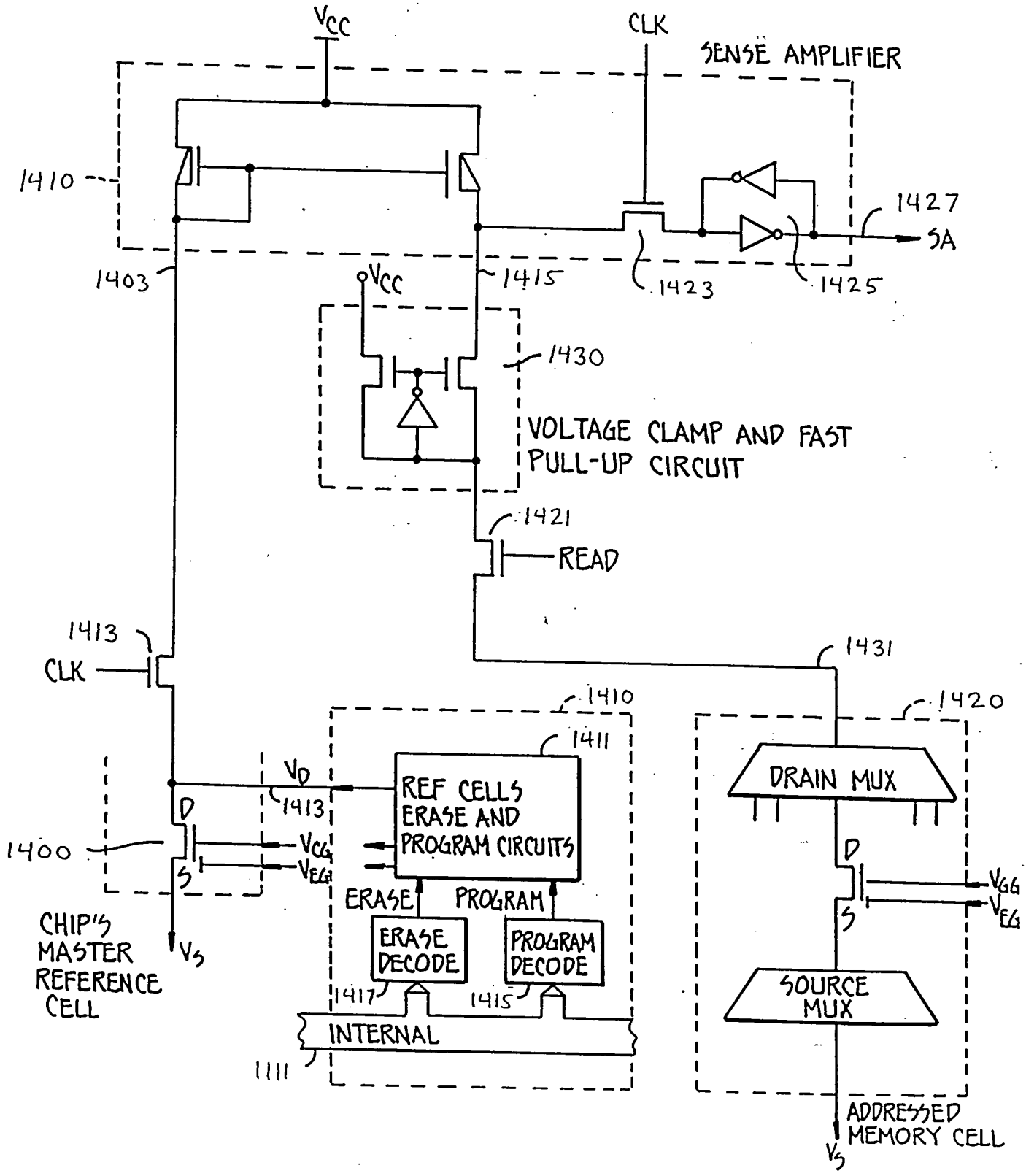

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{GG}
V_{EG}
S
ERASE
PROGRAM
V_{GG}
V_{EG}
S
CHIP'S MASTER REFERENCE CELL
V_S
ERASE DECODE
PROGRAM DECODE
SOURCE MUX
1417
1415
INTERNAL
1111
ADDRESSED MEMORY CELL
V_S

FIG. 17A

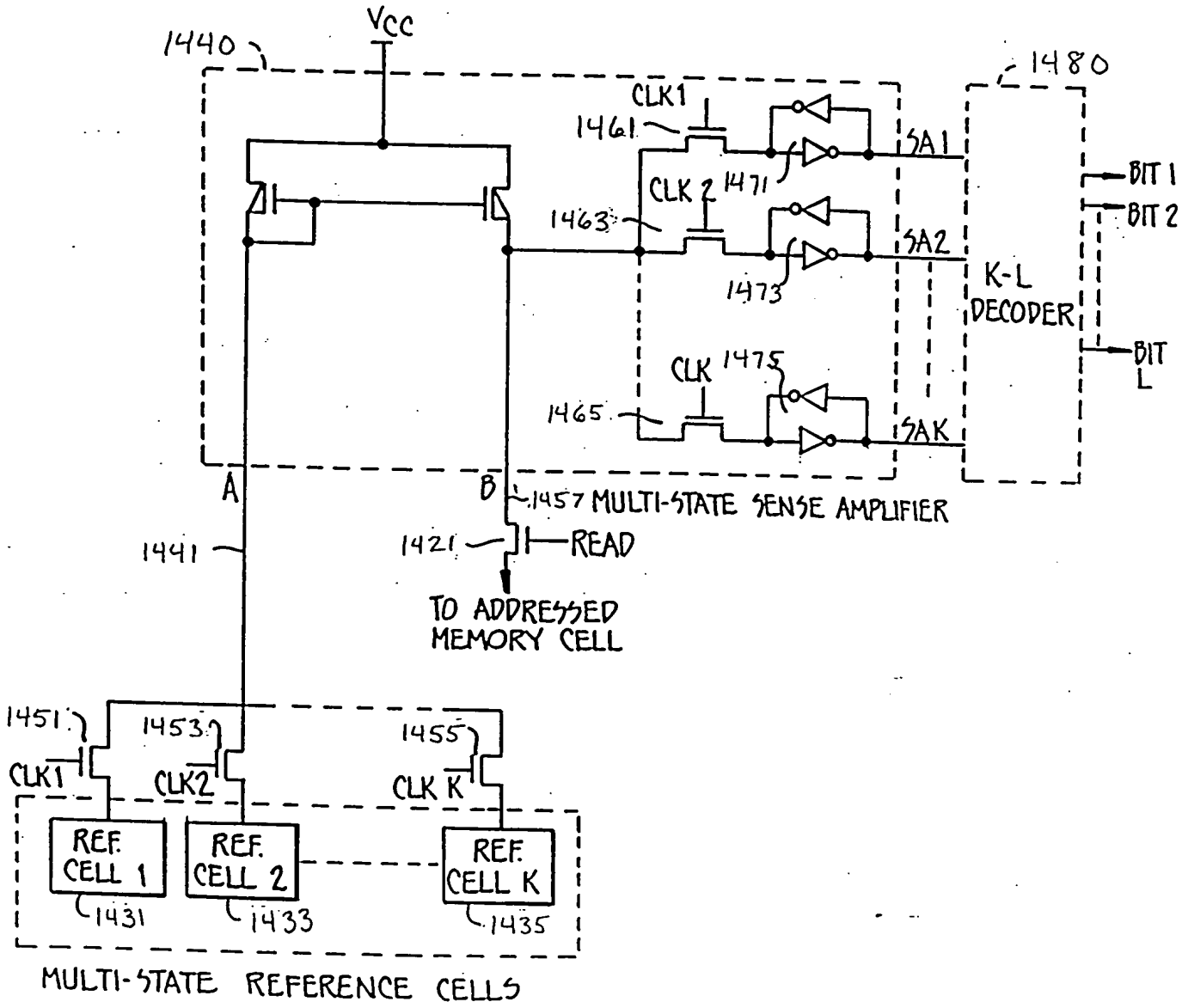

1440
Vcc
1480
CLK1
1461
SA1
BIT 1
CLK 2
1471
1463
SA2
BIT 2
K-L
DECODER
1473
CLK
1475
BIT
L
1465
SAK
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1441
1421
READ
TO ADDRESSED
MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG. ~~8B~~ 17B

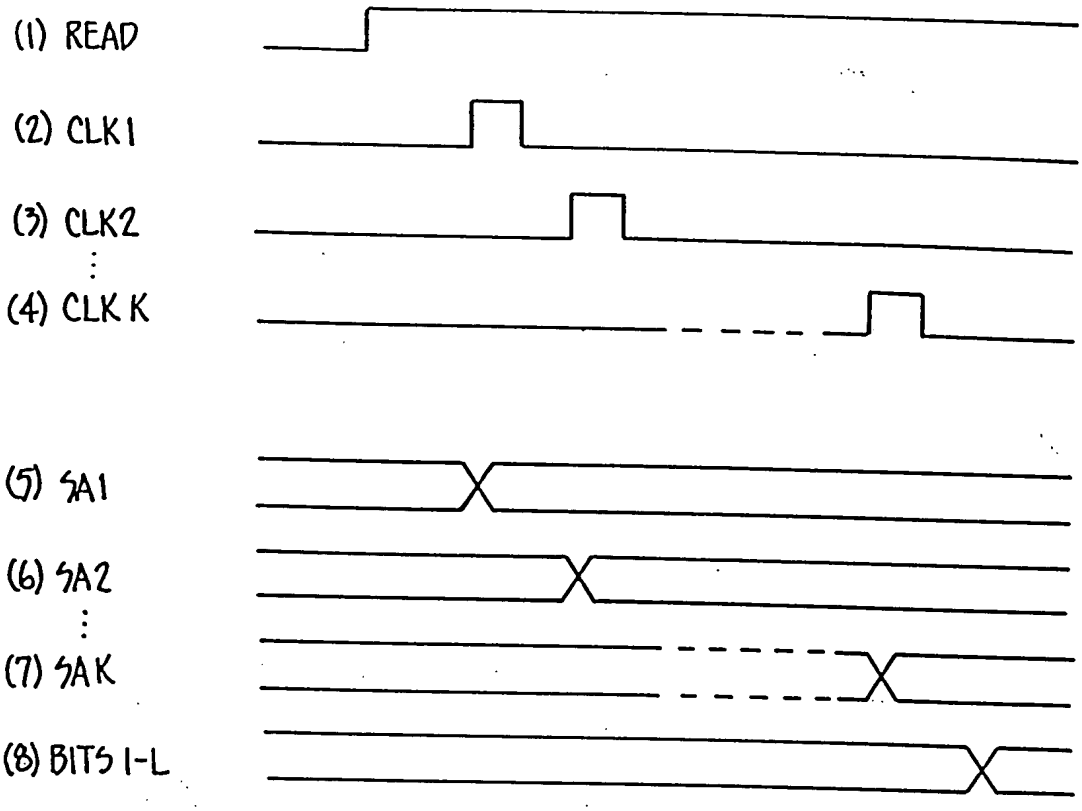


FIG. 17C

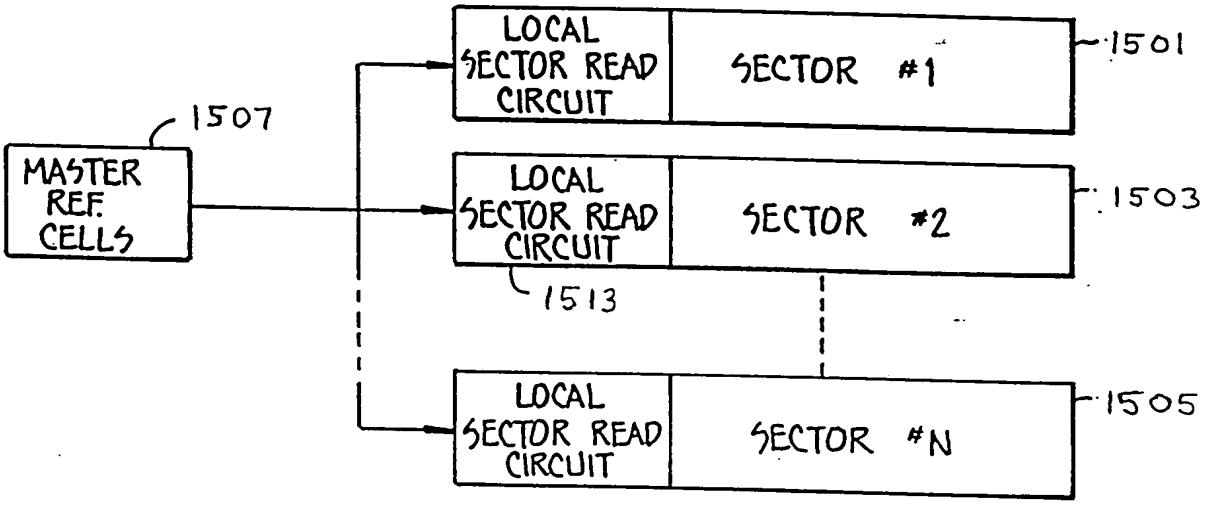


FIG. 18

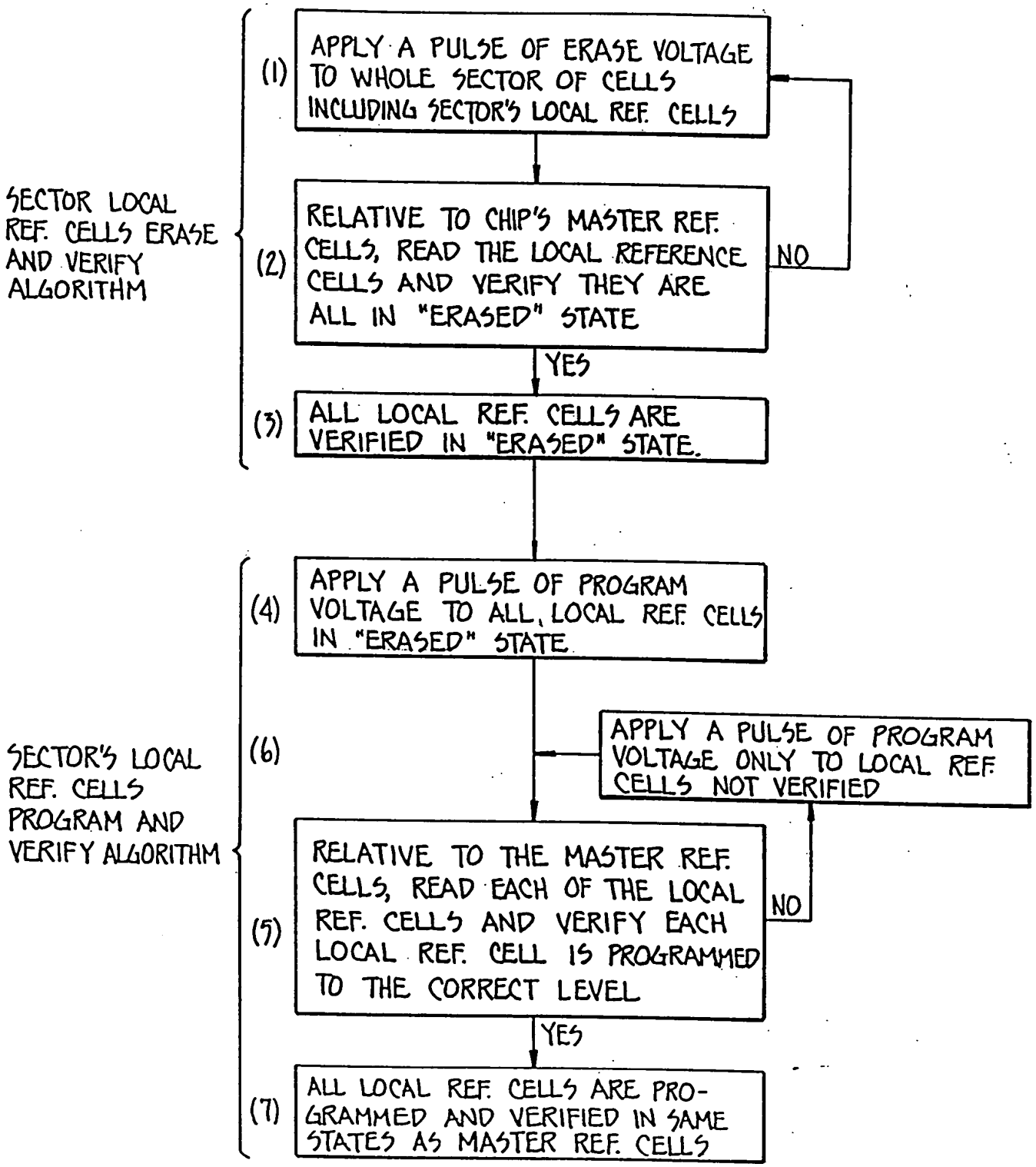

SECTOR LOCAL REF. CELLS ERASE AND VERIFY ALGORITHM
(1) APPLY A PULSE OF ERASE VOLTAGE TO WHOLE SECTOR OF CELLS INCLUDING SECTOR'S LOCAL REF. CELLS
(2) RELATIVE TO CHIP'S MASTER REF. CELLS, READ THE LOCAL REFERENCE CELLS AND VERIFY THEY ARE ALL IN "ERASED" STATE
NO
YES
(3) ALL LOCAL REF. CELLS ARE VERIFIED IN "ERASED" STATE.
SECTOR'S LOCAL REF. CELLS PROGRAM AND VERIFY ALGORITHM
(4) APPLY A PULSE OF PROGRAM VOLTAGE TO ALL LOCAL REF. CELLS IN "ERASED" STATE
(6) APPLY A PULSE OF PROGRAM VOLTAGE ONLY TO LOCAL REF. CELLS NOT VERIFIED
(5) RELATIVE TO THE MASTER REF. CELLS, READ EACH OF THE LOCAL REF. CELLS AND VERIFY EACH LOCAL REF. CELL IS PROGRAMMED TO THE CORRECT LEVEL
NO
YES
(7) ALL LOCAL REF. CELLS ARE PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

FIG. # 19

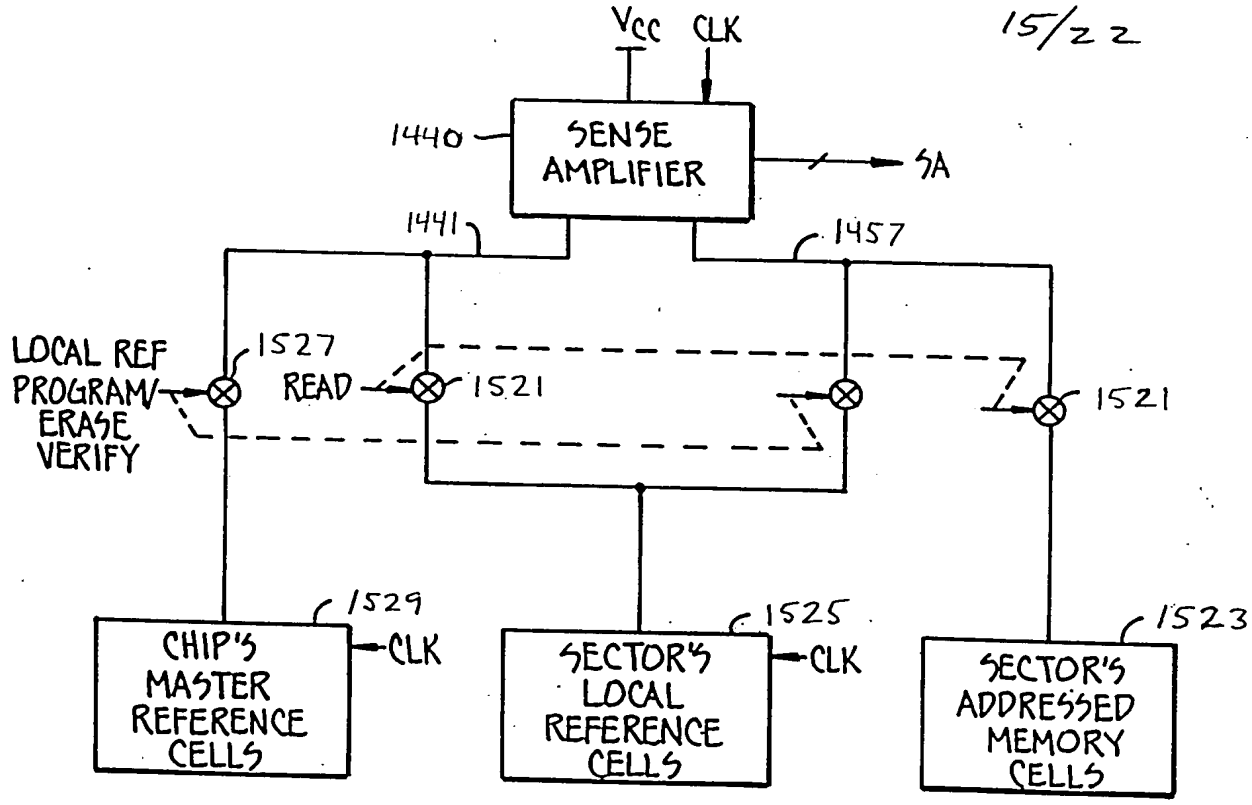


FIG. ~~12A~~ 20A

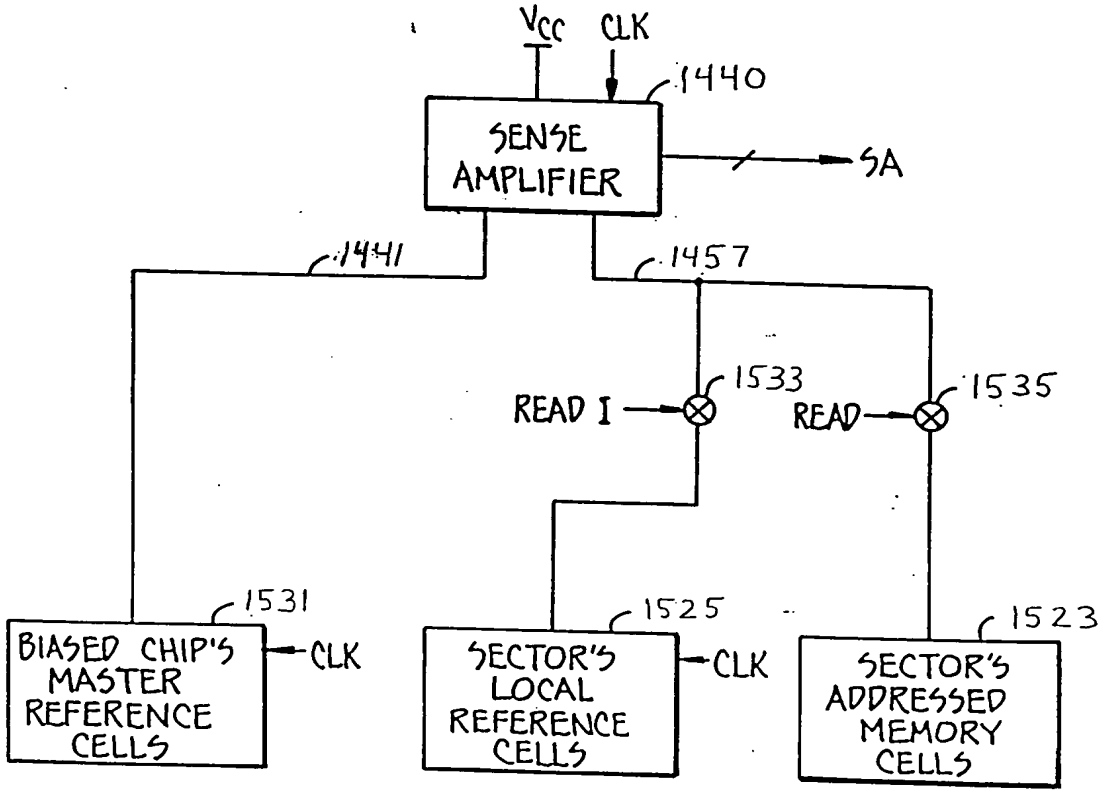


FIG. ~~13A~~ 21A

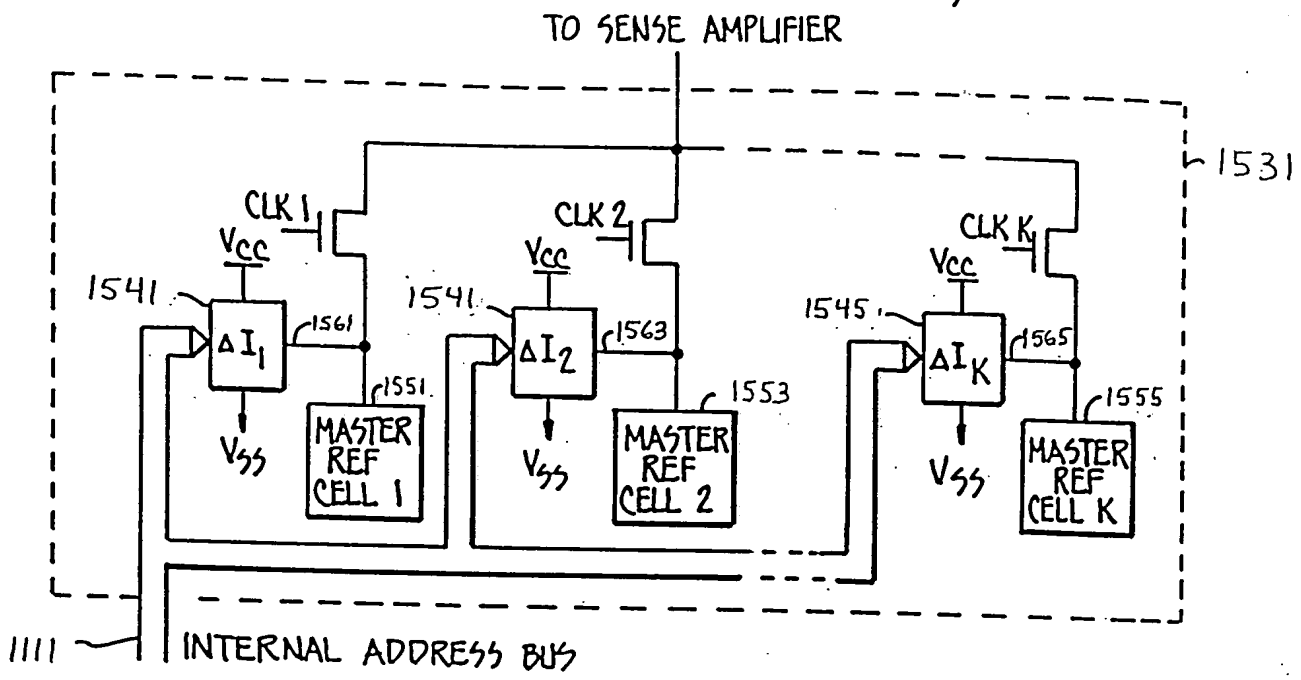


FIG. 21B

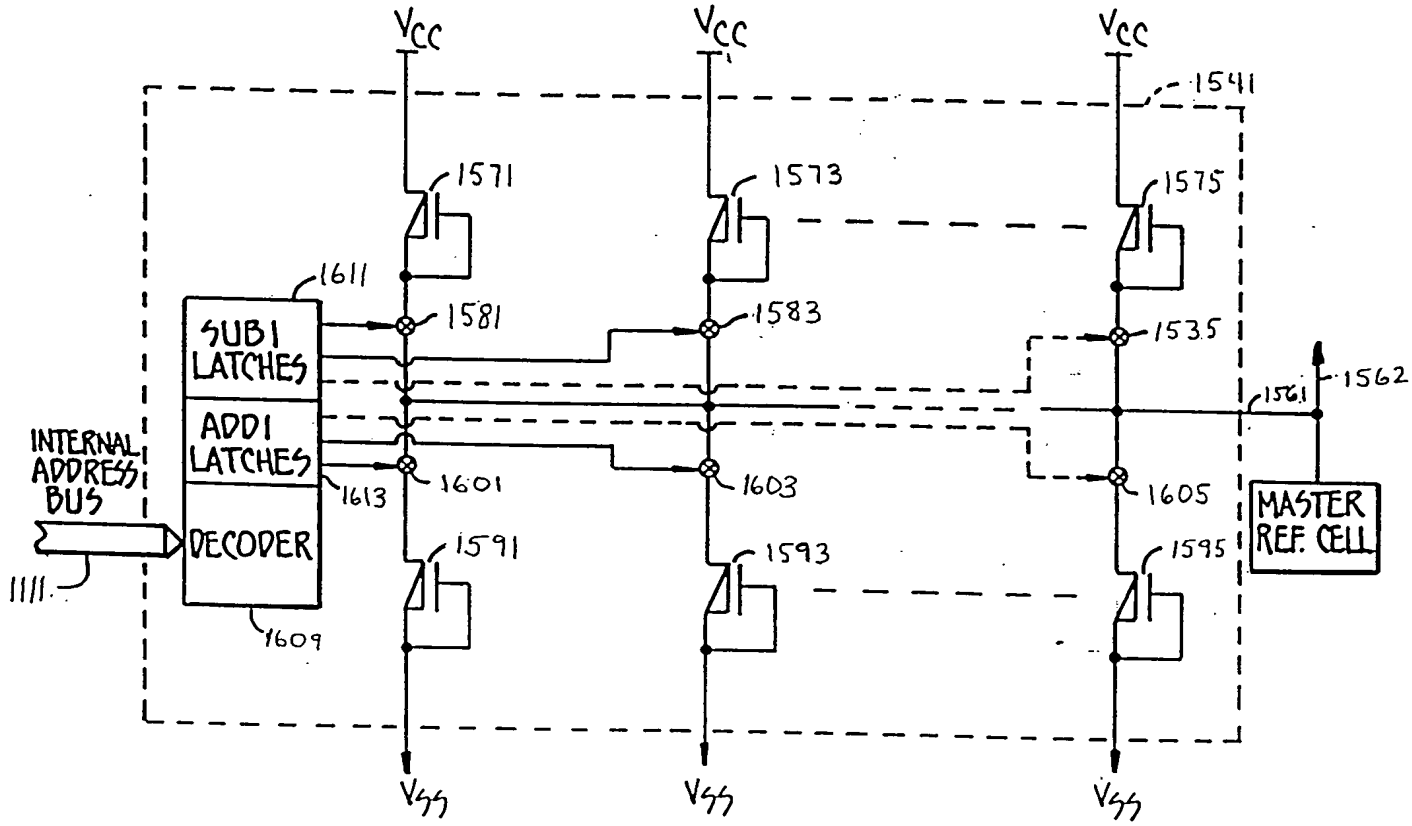


FIG. 21C

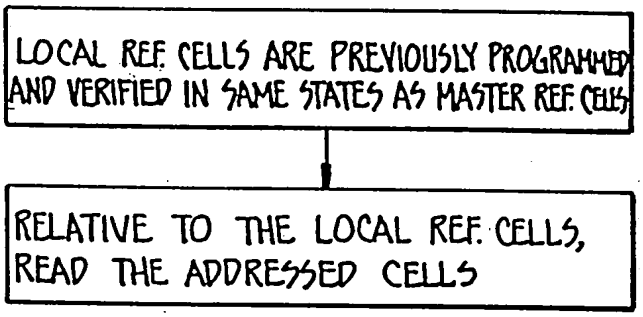


FIG. ~~12B~~ 20B

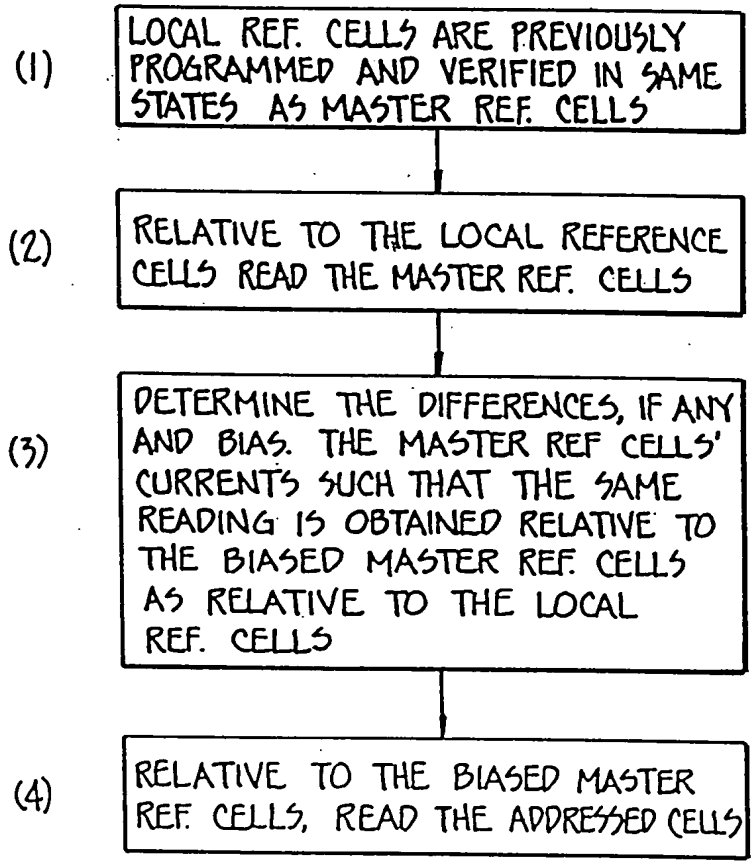
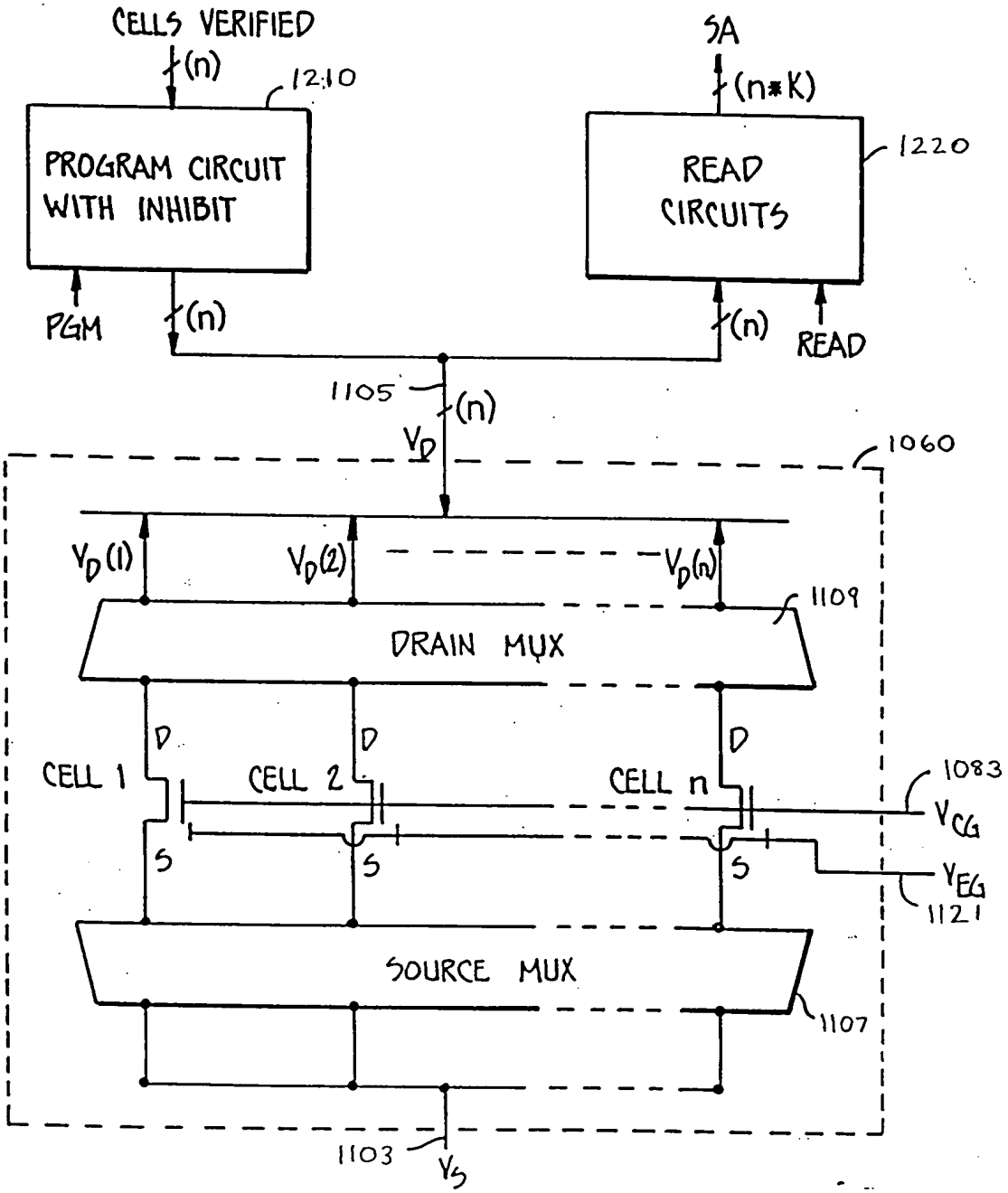
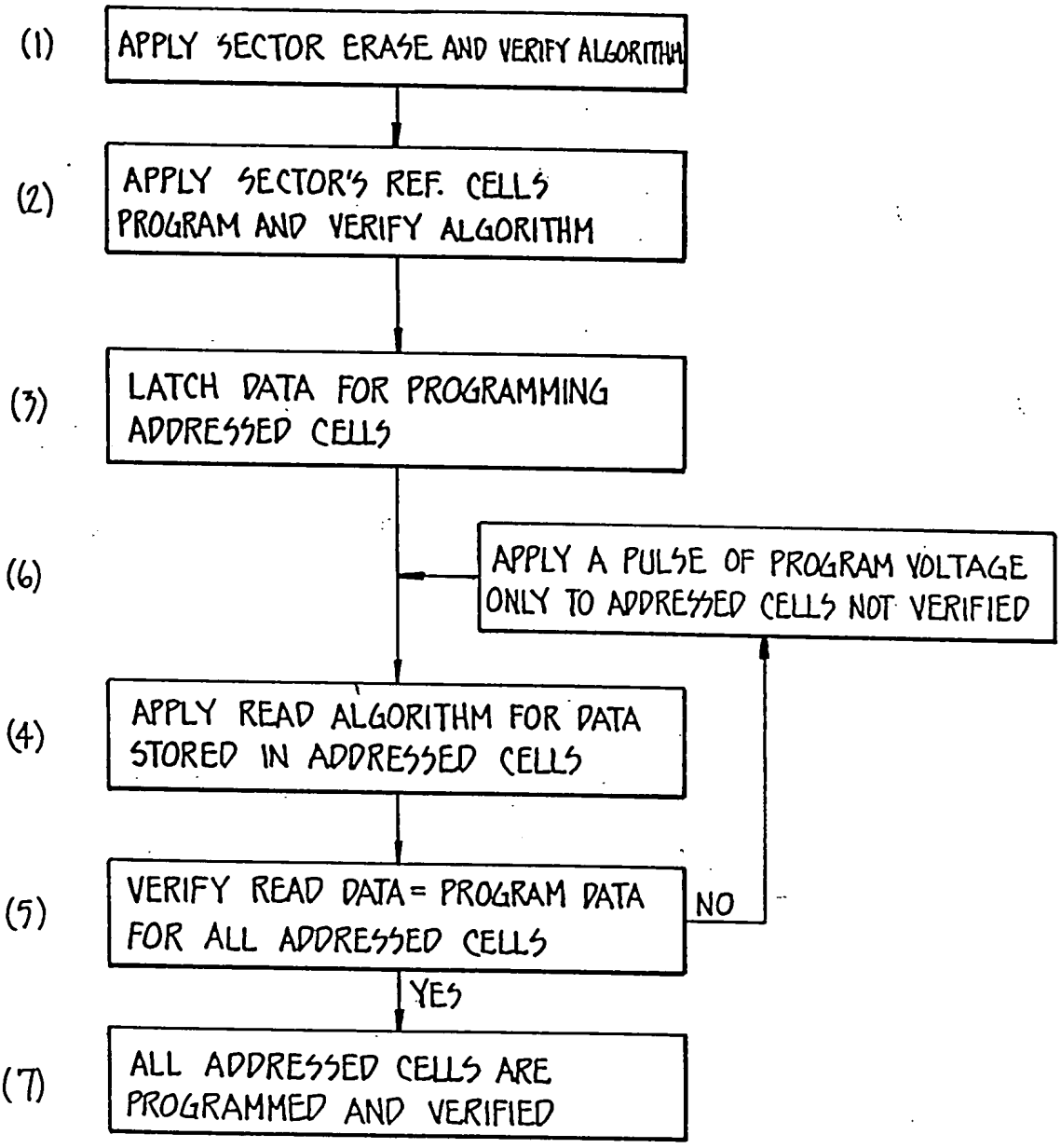


FIG. ~~13D~~ 21D



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.



PROGRAM ALGORITHM

FIG. 15. 23

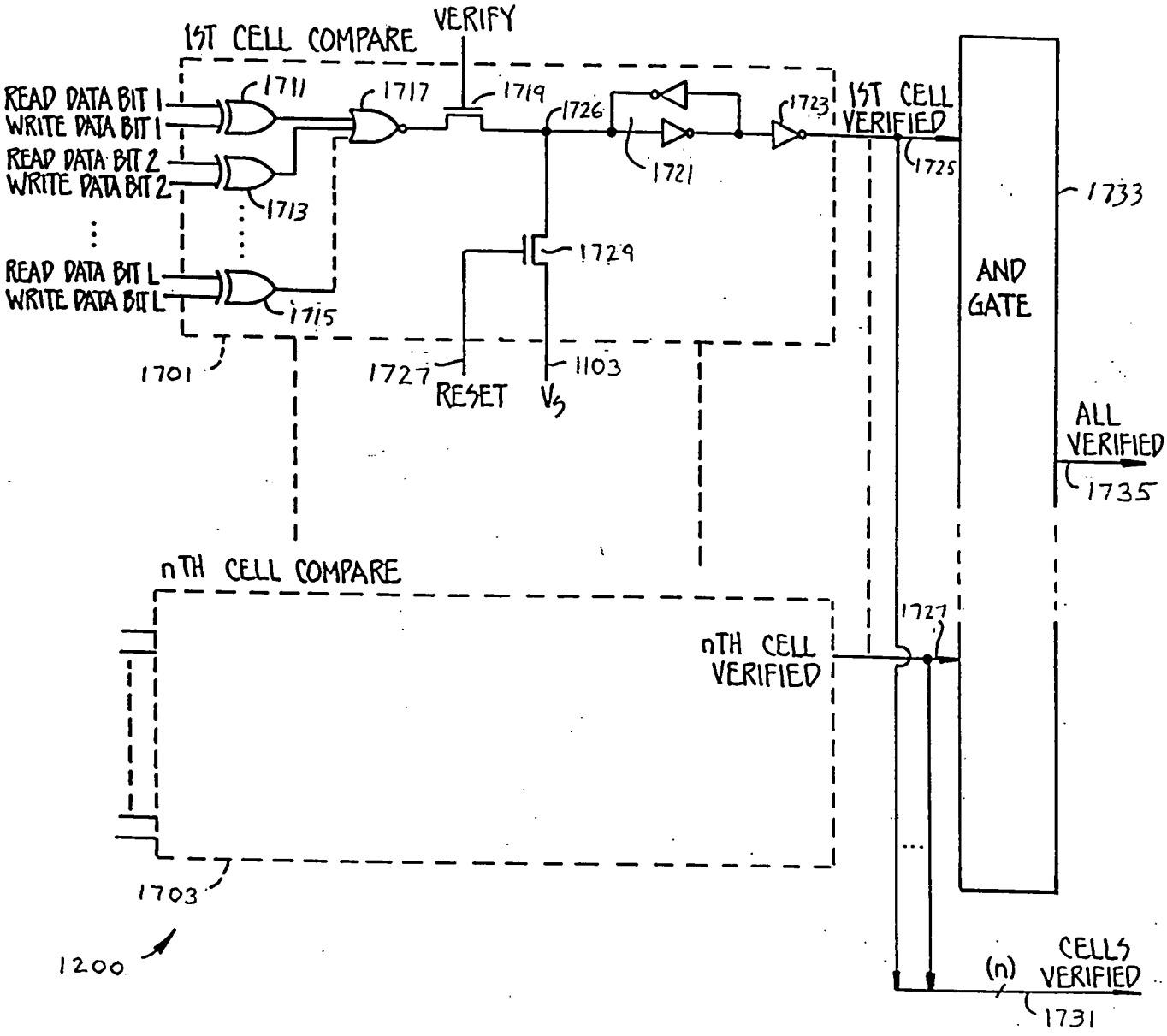

1ST CELL COMPARE
VERIFY
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
1711
1713
1715
1717
1719
1721
1723
1725
1726
1727
1729
1733
1735
1731
1701
1703
1200
1103
RESET
V_S
1ST CELL VERIFIED
AND GATE
ALL VERIFIED
nTH CELL COMPARE
nTH CELL VERIFIED
(n) CELLS VERIFIED

FIG. 24

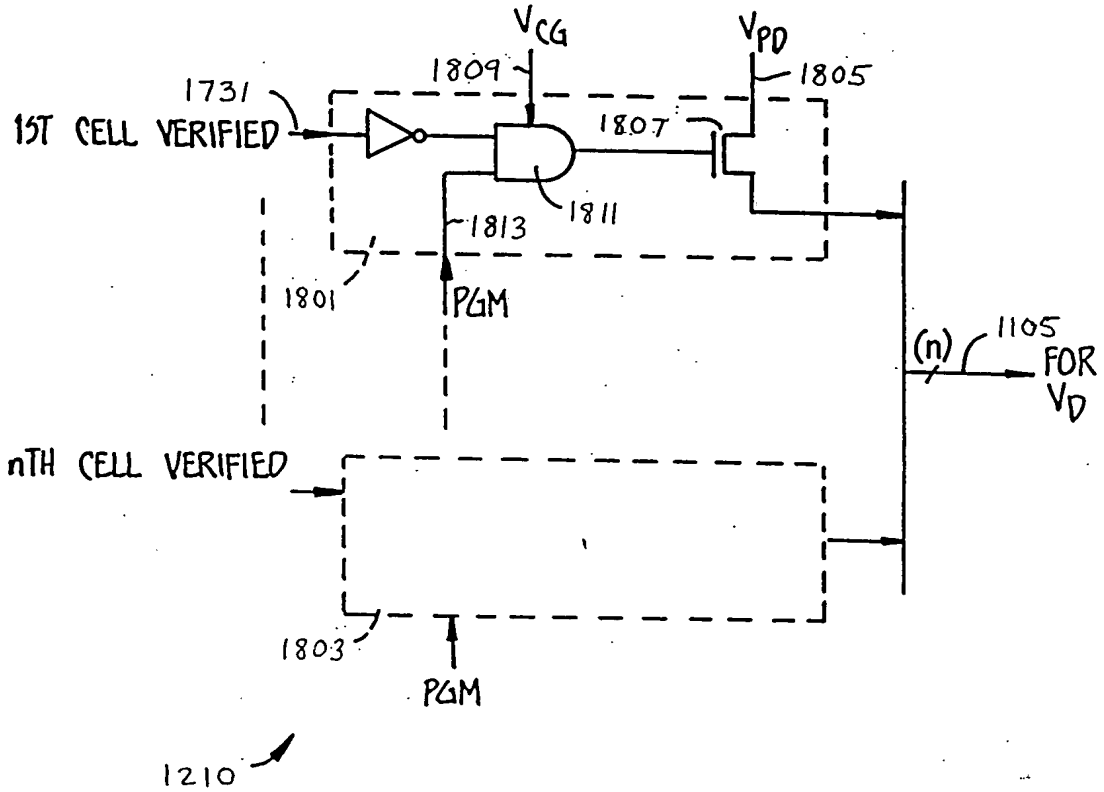

V_{CG}
V_{PD}
1809
1805
1731
1ST CELL VERIFIED
1807
1811
1813
1801
PGM
(n)
1105
FOR V_D
nTH CELL VERIFIED
1803
PGM
1210

FIG. 25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

~~TABLE 1~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12v	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5v	5v	5v	5v	5v
V_{PD}	V_{SS}	8v	8v	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20v	V_{SS}
unselected control gate	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
unselected bit line	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

~~TABLE 2~~ FIG. 27